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DEVELOPMENT OF MAGNETIC LOGIC BATCH FABRICATION TECHNIQUES

By C. H. Heckler Jr.
N. C. Bhiwandker

Prepared under Contract No. NAS1-7878 by
AMPEX CORP.
Redwood City, Calif.

for

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

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ABSTRACT

The process for making bimaterial multistage magnetic ferrite logic structures from the starting materials through the final firing cycle is described. The high coercive force material used in these structures has been developed to provide special partial set state magnetic characteristics. The second material was selected to have a low coercive force when bonded to, and fired with, the high coercive force material. The theory of operation of the multistage logic structures is discussed. The effect on operation due to use of materials having special partial set state characteristics and the use of low coercive force material for selected magnetic paths is described. Test results of the bimaterial multistage ferrite structures are given, together with operating data for 8-stage ring counters, each built from two bimaterial multistage logic structures. A process for plating low resistance conductors on ferrite logic structures was developed. These conductors are joint free and can be made to form multiple turns through apertures 0.040" in diameter. Test results on ten structures with two-turn plated 0.004" copper conductors are presented.

ACKNOWLEDGEMENTS

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CONTENTS

TABLES

FIGURES

1.0 INTRODUCTION

Under an earlier subcontract, Ampex developed for NASA Langley Research Center a process for making toroidal cores with special partial set state magnetic characteristics for use in magnetic logic circuits. An investigation was also made into the feasibility of making complex ferrite structures which would replace the multiple toroids that formed each logic stage in the toroidal magnetic circuits. This goal necessitated combining compositionally different ferrite materials within one structure to provide a low coercive force in selected magnetic paths. A process for combining compositionally different materials was developed, and multistage structures were integrated from a high and a low coercive force material. These structures were not perfect, due to warping and shape distortion. However, they did demonstrate the feasibility of combining two materials having different compositions and magnetic characteristics within a ferrite structure. Two such structures are functionally equivalent to 80 toroidal cores.

In the present program the goals have been: to eliminate the warping and distortion, to make and test a quantity of multistage integrated structures, to fabricate and evaluate ring counters made from these integrated structures, to design, make, and test a quantity of reduced-size integrated structures, to fabricate and evaluate ring counters made from the reduced-size structures, to investigate processes for applying conductor patterns to logic structures, to design an arithmetic unit based on the integrated structures, and to design, fabricate, and test those logic structures needed to realize the special logic functions required by the arithmetic unit design.

2.0 SUMMARY

During this program the problems associated with making multistage integrated logic structures were investigated. The doctor blade process of preparing the flexible sheets of ferrite from which the multistage structures were punched was replaced with a thermobonding method due to problems of yield and uniformity. Warping has been eliminated and the distortions minimized in the full-size structures. A new design was made for a reduced-size multistage integrated structure, and a molding process was developed to form these reduced-size structures. Full-size and reduced-size multistage integrated structures were fabricated and tested. Registers and ring counters constructed from these structures have been tested and evaluated. Good signal-to-noise ratios and operating ranges were obtained.

A plating process for applying two-turn conductor patterns through the output aperture of single-stage structures was developed. The process developed for plating conductor patterns has also been used to plate eddy current shields to reduce leakage flux in the logic structures.

An arithmetic unit has been designed based on the multistage integrated logic structures. A special structure to form the "exclusive-OR" function has been designed, fabricated, and tested.

3. FERRITE MATERIALS

3.1 Powder Processing

Preparation of ferrite powders for the integrated ferrite logic structures made under this program has followed standard ceramic processing techniques up to the point of binder addition. The initial process used for making full-size integrated logic structures is shown in the process flow chart, Fig. 1. The starting materials are reagent grade oxides and carbonates. The assays and spectrographic analyses for these starting materials are given in Appendix II. The high H_c and low H_c compositions used in the full-size structures are listed in Table 1. These compositions were found to have the desired magnetic characteristics in an earlier contract.[1]

The materials are wet-mixed, after weighing, by ball-milling for 16 hours to form a homogeneous mixture. The mixture is dried and calcined to convert the carbonates to oxides. The high H_c material IS25 is calcined at 1050°C. The low H_c material IS40 is calcined at 950°C. After calcining, the powders are ball-milled to reduce the particle size, then dried and screened preparatory to the addition of binder. The number and sequence of process steps carried out in the preparation of both high and low H_c powders are the same.

3.2 Sheet Forming

The binders used are thermoplastic and are formulated to yield flexible sheets. Two methods of sheet formation have been used. The original method was to cast sheets by the doctor-blade process. Here the binder constituents, solvent, and calcined ferrite powder are weighed out and mixed by ball-milling for 16 hours to obtain a homogeneous dispersion

of the ferrite powder in the binder solution, ie, a slurry. The slurry is poured from the ball mill in which it was mixed into a container which is then placed in a vacuum chamber. As the chamber is evacuated, entrapped air is eliminated from the slurry. The slurry is then poured onto a casting

High H_c Material	Low H_c Material
Weighing	Weighing
Oxides	Oxides
Carbonates	Carbonates
Mixing	Mixing
Drying	Drying
Calcining	Calcining
Ball Milling	Ball Milling
Drying	Drying
Screening	Screening
Weighing	Weighing
Ferrite	Ferrite
Binder Constituents	Binder Constituents
Mixing	Mixing
Sheet Casting	Sheet Casting
Drying	Drying
Preform Punching	Preform Punching

Assembly

Compression Bonding

Final Punching

Firing

Fig. 1 Flow Diagram - Process #1 (Full-Size Structures)

surface and is spread and leveled to the desired wet thickness by steadily drawing a doctor-blade through the poured slurry. When dry, the flexible sheets can be peeled from the casting surface. When relatively thick sheets are cast, ie, greater than 0.04", there is a strong tendency for the sheets to crack during drying. Moreover, there is a tendency for the slurry to flow out from the edges while drying (ie, "slumping") which causes the dried sheets to be nonuniform in thickness. As a result of both the cracking and slumping, only selected portions of a cast sheet may be used. The rest is wasted material.

To correct these deficiencies a second sheet forming process was developed. In this process the slurry is poured directly from the mill into drying pans without going through the evacuation step. When dry, the material is scraped from the pan and broken up to form a powder by forcing it through a 20 mesh screen. This powder is bottled and stored for later use. The sheets are formed by pouring a measured quantity of the powder into a die which is then closed and placed on the heated plattens of a Carver hydraulic press. The sheet is formed by thermopressing at 85^{o}C and 4000 psi. The excess material is extruded out of the die and the thickness of the thermobonded sheet is controlled by limiting the penetration of the plunger with a shim. The sheet, when removed from the die, is solid, flexible, of uniform texture, and of a controlled uniform thickness.

3.3 Firing

A firing cycle was used in which the desired magnetic characteristics in both the high H_c and low H_c materials were obtained when fired together in the same firing. This is a necessary requirement, since the integrated structures contain both materials. The material characteristics of prime importance are: in the high H_c material the partial set state thresholds, and in the low H_c material the coercive force. Since the firing conditions required to obtain the desired partial set state characteristics in the high H_c material are quite restrictive, the approach taken was to find a low

coercive force composition which had a sufficiently low coercive force under these firing conditions.

Two firing cycles have been used to obtain the desired magnetic characteristics in the materials prepared during this program. The materials used in full-size structures have been fired in air at 1300°C for 4 hours. At the end of soak the atmosphere is switched to nitrogen for the cooling portion of the cycle. The cooling rate is 100°C per hour.

The materials used in the reduced-size structures have been fired in air at 1250°C for 4 hours. At the end of soak the atmosphere is switched to nitrogen for the cooling portion of the cycle. The cooling rate is 100°C per hour.

The magnetic characteristics obtained for the high and low H_c materials fired under the above conditions are given in Tables 2 and 3.

Table 1 Ferrite Compositions

FULL-SIZE STRUCTURES

High H_c formulation IS-25

$$Mg_{0.675}Mn_{0.525}Fe_{1.800}O_4$$

Low H_c formulation IS-40

$$Mg_{0.486}Mn_{0.528}Cd_{0.201}Fe_{1.780}O_4 + 0.25\%\ Ca\ (weight)$$

REDUCED-SIZE STRUCTURES

High H_c formulation IS-25 + ThO_2

$$Mg_{0.675}Mn_{0.525}Fe_{1.800}O_4 + 2\%\ ThO_2\ (weight)$$

Low H_c formulation IS-40

$$Mg_{0.486}Mn_{0.480}Cd_{0.250}Fe_{1.780}O_4 + 0.25\%\ Ca\ (weight)$$

Table 2 Material Characteristics for Multistage Structures

High H_c Material	Target	Achieved
H_c (oersteds)	1.8	2.2
B_r (gauss)	1700	1690
Squareness	$\geq$ 0.9	0.9
S_w (Oe -μ sec)	$\leq$ 1.0	0.6
Minor Loop Properties		
$\frac{TH_{ps}(50\%)}{TH}$	$>TH\ \frac{OD + ID}{2\ ID}$	$> TH\ \frac{OD + ID}{2\ ID}$
Low H_c Material		
H_c (oersteds)	$\leq$ 0.6	0.95
B_r (gauss)	1700	1830
Squareness	$\geq$ 0.9	0.93
S_w (Oe - μsec)	$\leq$ 1.0	0.6
Both High and Low H_c Materials		
Firing Temp & Atmosphere	Same	Same
Curie Temp	$>250^{\circ}C$	$>250^{\circ}C$
H_c ratio	$\geq$ 3:1	2.3:1

Table 3 Material Characteristics for Reduced-Size Structures

High H_c Material	Target	Achieved
H_c (oersteds)	4.2	3.5
B_r (gauss)	1700	1720
Squareness	≥ 0.90	0.95
S_w (Oe - μ sec)	≤ 1.0	0.6
Minor Loop Properties		
$\frac{TH_{ps}(50\%)}{TH}$	$> TH \frac{OD + ID}{2\ ID}$	$> TH \frac{OD + ID}{2\ ID}$
Low H_c Material		
H_c (oersteds)	≤ 0.6	1.7
B_r (gauss)	1700	1783
Squareness	≥ 0.90	0.92
S_w (Oe - μsec)	≤ 1.0	0.6
Both High and Low H_c Materials		
Firing Temp & Atmosphere	Same	Same
Curie Temperature	$>250^{\circ}C$	$>250^{\circ}C$
H_c ratio	$\geq 7:1$	$> 2:1$

4.0 INTEGRATED FERRITE LOGIC STRUCTURES

4.1 Structure Preparation

4.1.1 Punching

The full-size integrated logic structures have been prepared by die punching from bimaterial sheets. Originally, the high H_c and low H_c sheets were cast by the doctor-blading process. Later the thermopressing process described in Section 3.2 was used. The complete processes used to make the full-size integrated logic structures are shown in the flow diagrams of Fig. 1 and Fig. 2 and the method of making these structures is depicted in Figs. 3 and 4. In the doctor-blade process, 3.3 inch by 0.75 inch punching blanks are cut from the cast sheets. The thermopressed punching blanks are formed into this size directly from the powder.

The bimaterial sheets are formed by punching both a high H_c and a low H_c punching blank in the insert-punching die. The high H_c punchouts are discarded. The low H_c punchouts are inserted in the holes punched out of the high H_c punching blank.

The high H_c punching blank, with low H_c inserts in place, is placed in a thermobonding die. The die is seated on the heated plattens of a hydraulic press and stabilized at 85°C. A pressure of 4000 psi is then applied to produce thermoplastic flow thereby bonding the interfaces and forming a unitized bimaterial punching blank. The bimaterial punching blank is then positioned in the punching die, so that the low H_c inserts are located over the output aperture in each stage. The structure shown by the outline in Fig. 3 is then punched out of the bimaterial blank and removed from the die. The structures are placed on an alumina setter for firing. An intervening layer of fine thoria powder is used to prevent sticking to the setter.

Certain problems resulted from preparations of structures by punching. These were:

(1) Irregular sheared surfaces occurred which resulted in varying

High H_c Material	Low H_c Material
Weighing	Weighing
Oxides	Oxides
Carbonates	Carbonates
Mixing	Mixing
Drying	Drying
Calcining	Calcining
Ball Milling	Ball Milling
Drying	Drying
Screening	Screening
Weighing	Weighing
Ferrite	Ferrite
Binder Constituents	Binder Constituents
Mixing	Mixing
Drying	Drying
Screening	Screening
Sheet Molding	Sheet Molding
Preform Punching	Preform Punching

Assembly

Compression Bonding

Final Punching

Firing

Fig. 2 Flow Diagram - Process #2 (Full-Size Structures)

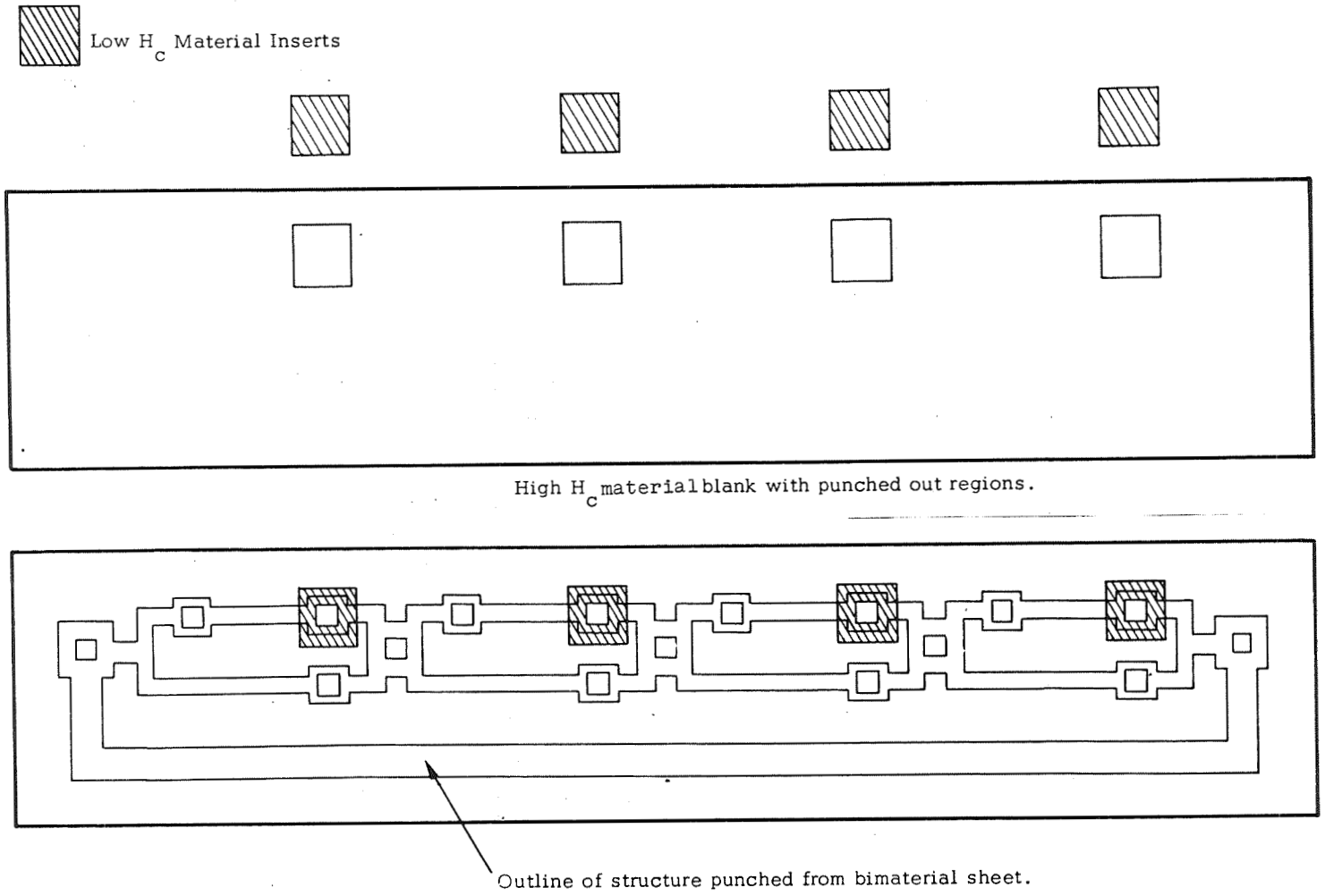


Fig. 3 Method of Preparing Bimaterial Integrated Multistage Logic Structures

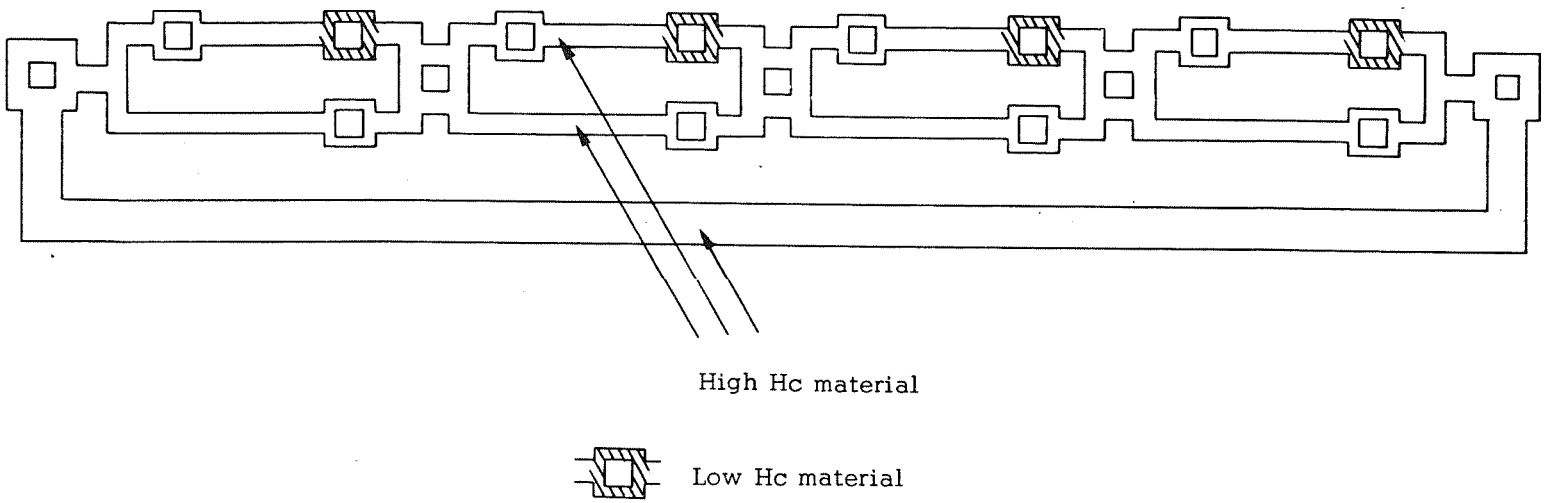


Fig. 4 Integrated Multistage Logic Structure Showing Low H_c Inserts

cross sectional areas of the legs.

(2) The pressure required to punch out structures produced plastic flow and caused shape distortion.

(3) Die modification was not possible.

4.1.2 Molding

The reduced-size structures have been prepared by a molding process developed to overcome the problems encountered in punching the full-size structures. The mold was prepared from stainless steel, using a three-dimensional engraver's pantograph. This mold, and the insert punching die, are shown in Figs. 5 and 6. The complete process for making reduced-size structures is shown in the flow diagram of Fig. 7.

The molding of structures is made possible because of the thermoplastic property of the binder system, the same property which produces the bonding between the high and low H_c materials. The methyl methacrylate binder system is used for molding structures because of its characteristic of superior release from the metal surfaces of the mold.

The molding blank for the reduced size structure is smaller but it is prepared in the same manner as the punching blank for the full-size structures. The high H_c and low H_c materials are separately punched in the insert punching die. The low H_c punchouts are inserted in the punched out holes in the high H_c molding blank. This blank is placed in the thermopressing die and thermobonded at 90°C and 5000 psi to form a unitized bimaterial molding blank.

To accomplish the molding, the bimaterial molding blank is positioned on the mold such that the low H_c inserts are over the output aperture in each stage. The top of the mold is added and the mold is placed on the heated plattens of the hydraulic press and stabilized at 90°C. A force of 1000 pounds is applied to cause the material to flow into the mold.

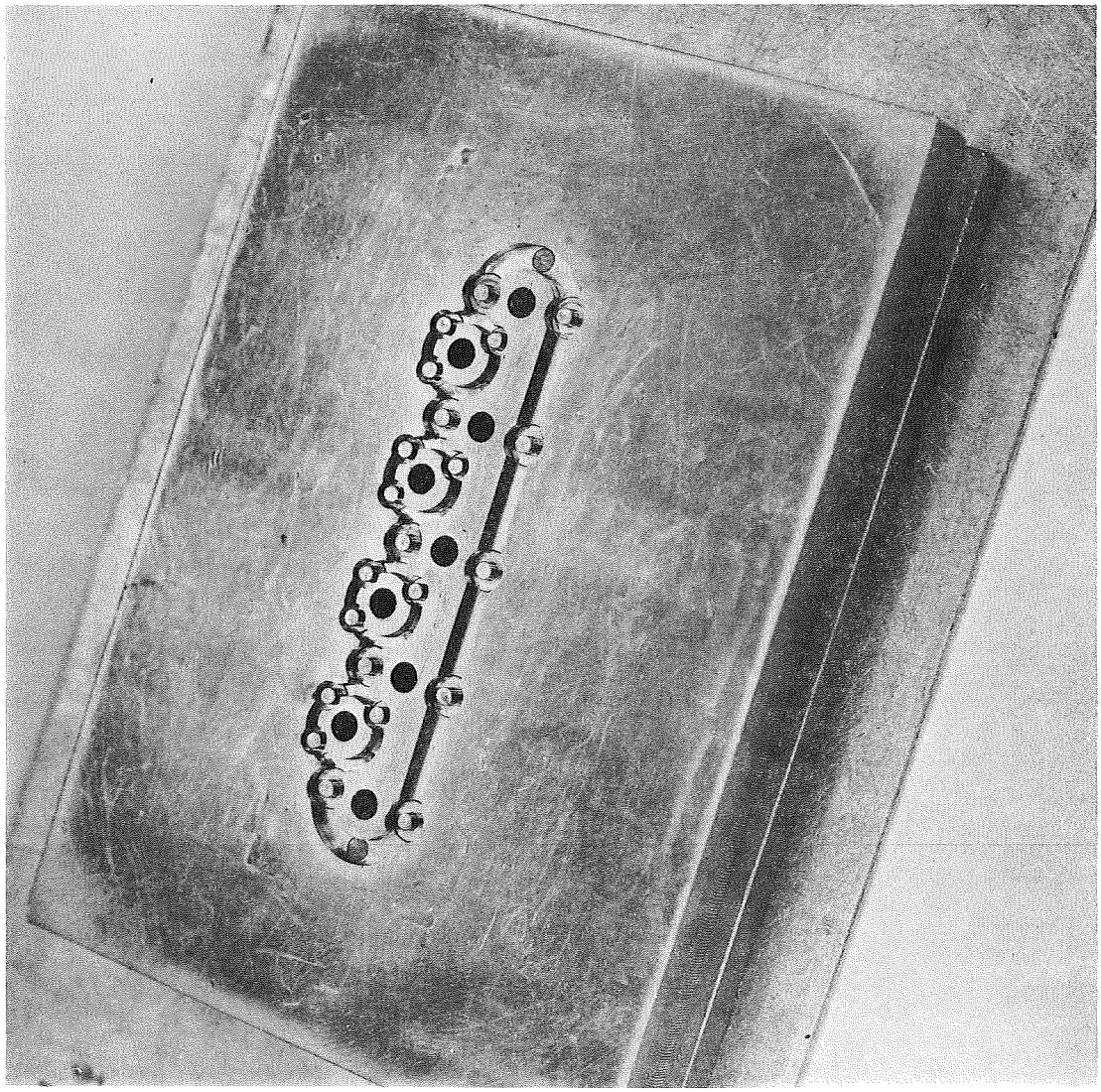


Fig. 5 Mold for Reduced-Size Integrated Multistage Logic Structures

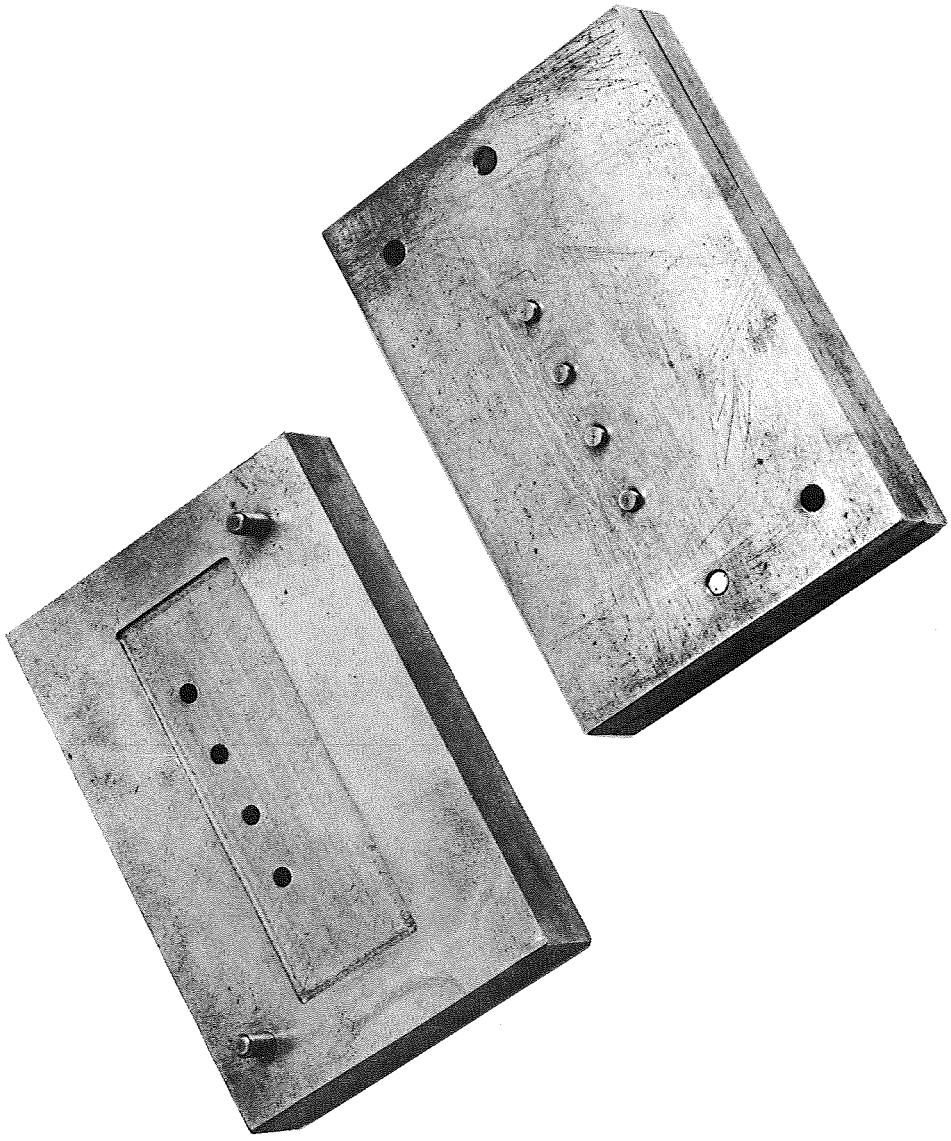


Fig. 6 Insert Punching Die for Reduced-Size Integrated Multi-Stage Logic Structures

High H_c Material	Low H_c Material
Weighing	Weighing
Oxides	Oxides
Carbonates	Carbonates
Mixing	Mixing
Drying	Drying
Calcining	Calcining
Ball Milling	Ball Milling
Drying	Drying
Screening	Screening
Weighing	Weighing
Ferrite	Ferrite
Binder Const.	Binder Const.
Mixing	Mixing
Drying	Drying
Screening	Screening
Sheet Molding	Sheet Molding
Preform Punching	Preform Punching

Assembly

Compression Bonding

Final Molding

Firing

Fig. 7 Flow Diagram - Process #3 (Reduced-Size Structures)

The pressure involved in this operation is less than 8000 psi. The molded structure is ejected from the mold after it cools to room temperature (Fig. 8) and placed on an alumina setter for firing. An intervening layer of fine thoria powder is used to prevent sticking during firing.

The same process is used to mold exclusive-OR logic structures. The mold and an ejected exclusive-OR structure are shown in Figs. 9 and 10.

4.1.3 Firing

The firings of all the integrated logic structures have been made in a laboratory tube furnace equipped for atmosphere firing. The firing schedule used for each of the structures is shown in Table 4. A flowing atmosphere at a rate of approximately 10 furnace volumes per hour is used throughout the firing.

Table 4 Firing Schedules

FULL-SIZE INTEGRATED LOGIC STRUCTURES

Heating: 35°C/hr in a flowing air atmosphere

Soak: 4 hours at 1300°C in a flowing air atmosphere

Cool: 100°C/hr in a flowing nitrogen atmosphere

REDUCED-SIZE INTEGRATED LOGIC STRUCTURES

Heating: 35°C/hr in a flowing air atmosphere

Soak: 4 hours at 1250°C in a flowing air atmosphere

Cool: 100°C/hr in a flowing nitrogen atmosphere

EXCLUSIVE-OR LOGIC STRUCTURES

Heating: 35°C in a flowing air atmosphere

Soak: 4 hours at 1250°C in a flowing air atmosphere

Cool: 100°C/hr in a flowing nitrogen atmosphere

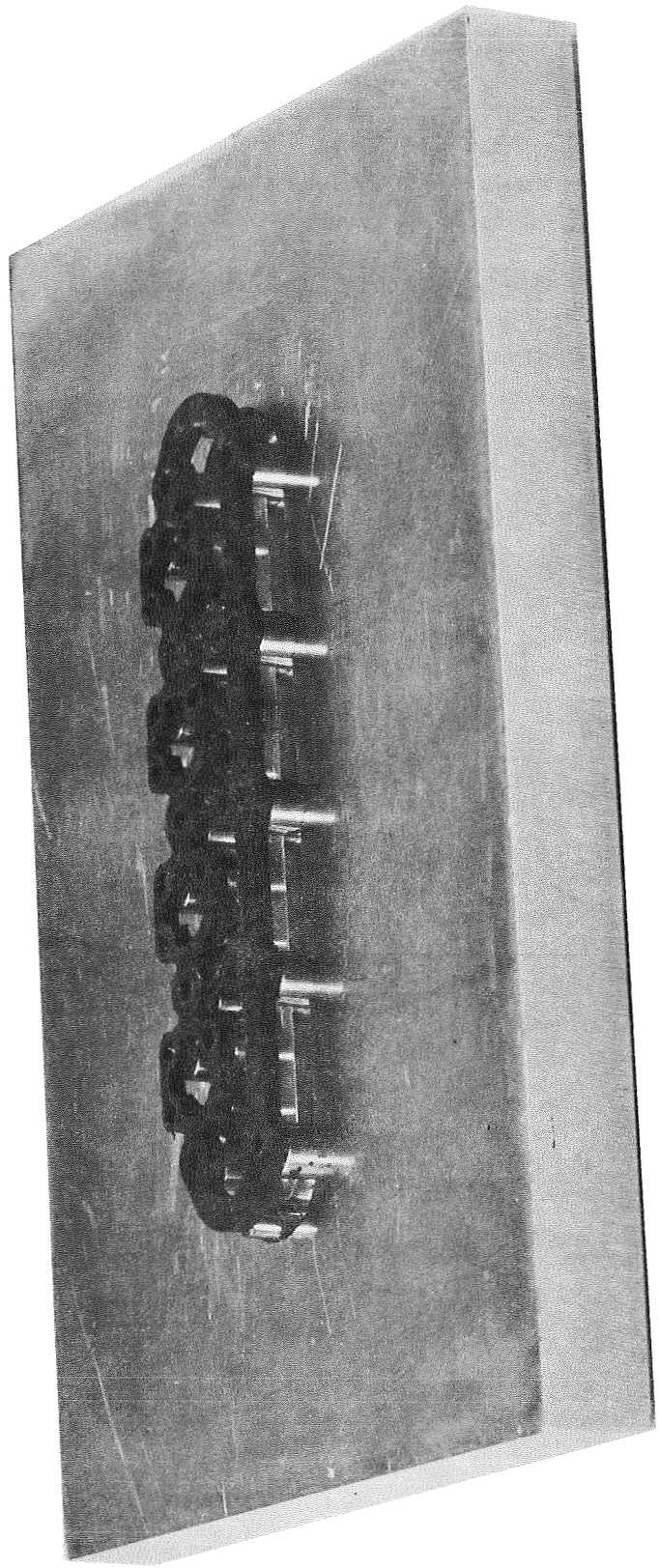


Fig. 8 Ejected Reduced-Size Logic Structure on the Mold

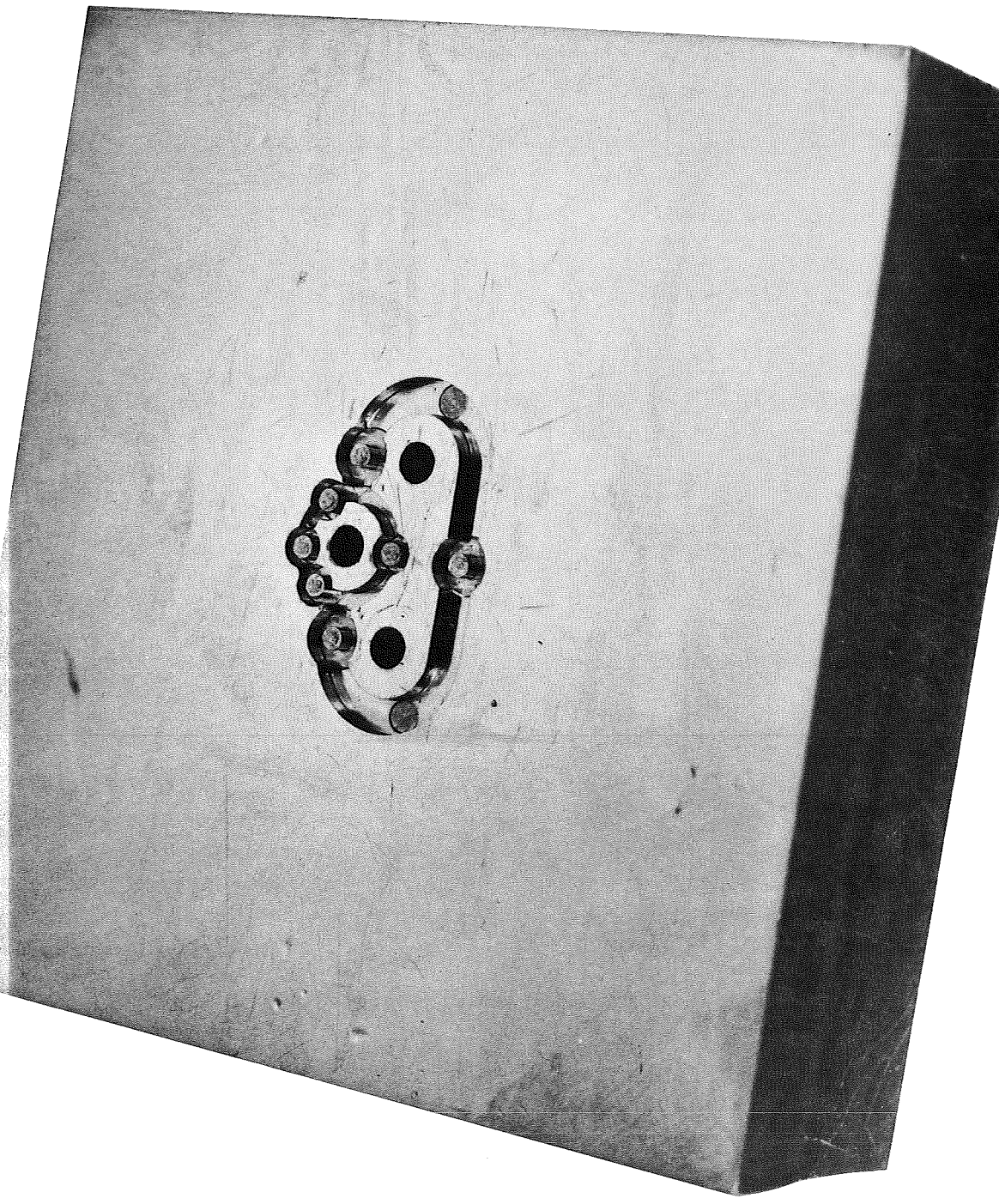


Fig. 9 Mold for Exclusive-OR Logic Structure

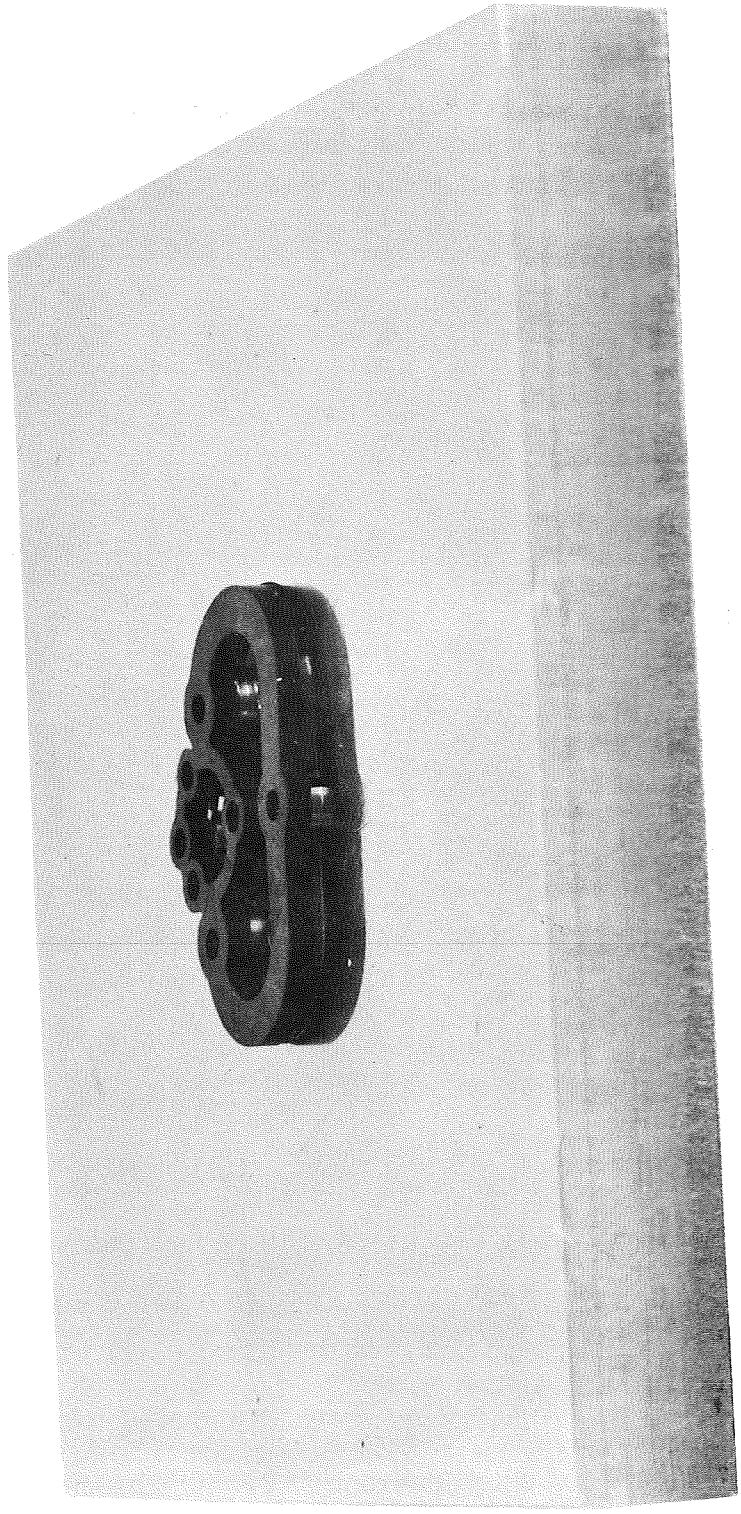


Fig. 10 Ejected Exclusive-OR Logic Structures on the Mold

4.2 Theory of Operation

4.2.1 Description of Operation

The theory of operation of the full-size and reduced-size integrated logic structures is the same. The physical differences between the two structures have been designed to improve performance. To simplify the description of operation, the single-stage structure shown in Fig. 11 will be discussed. Each stage in a multistage structure functions the same as does the stage of the single-stage structure. As seen in Fig. 11, the stage consists of the following magnetic paths: leg A, leg B, legs 1 and 2 of the input aperture, legs 1 and 2 of output aperture A, and legs 1 and 2 of output aperture B. The return leg in both the multistage and single stage structures is used to provide a flux path for the clear state flux pattern.

The flux states of each leg are shown, for the clear state, in Fig. 12a. Note that each leg is saturated in a counterclockwise direction with respect to the main aperture. The cross sectional areas of the legs are proportioned such that when both legs of an aperture are saturated in the same direction then the leg contiguous to this aperture is also saturated. Circuit operation[∓] is based on a four-clock cycle. At the first clock time the structure is set in its clear state. At the second clock time the even-to-odd advance-drive pulse occurs and information is transferred into the stage. At this advance time, current through the flux drive winding switches flux in a clockwise direction around the main aperture. The amount of flux switched, however, is limited by the pattern of the flux drive winding. Current through this "figure eight" winding will switch only one leg of the drive apertures from the clear state. The other leg is driven in the clear state direction. Therefore one half of the flux capacity*

*The flux in each leg when in the clear state is $-\phi_r$ and when fully reversed or in the set state the flux is $+\phi_r$. This difference, $2\phi_r$, is the maximum flux which can be irreversibly switched and is here called the flux capacity of a leg.

∓ The windings are positioned as shown for the reduced size structures in Fig. 23.

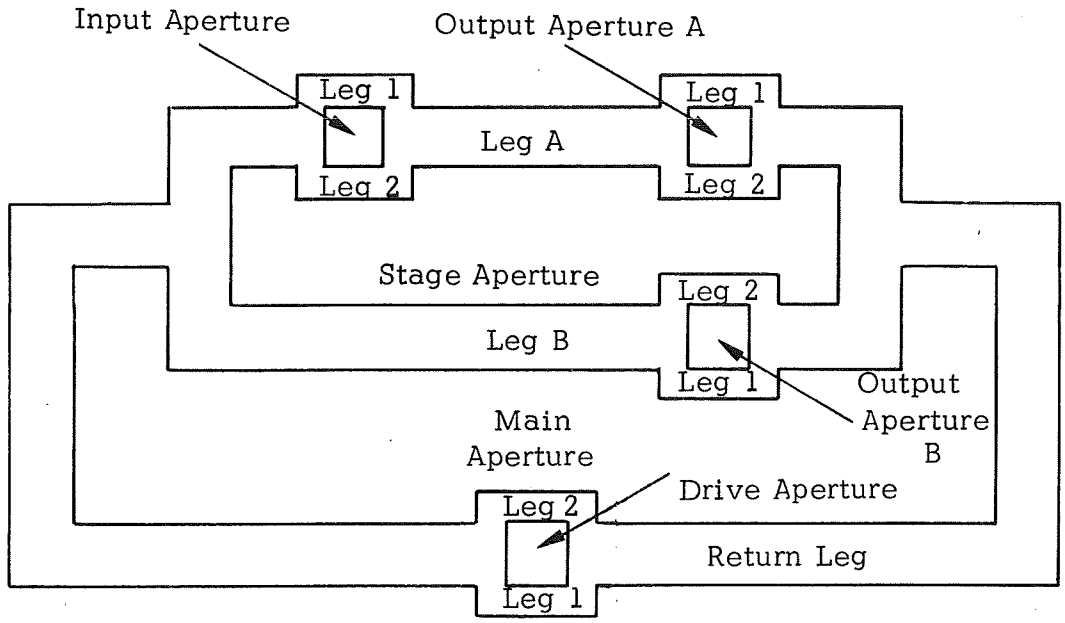
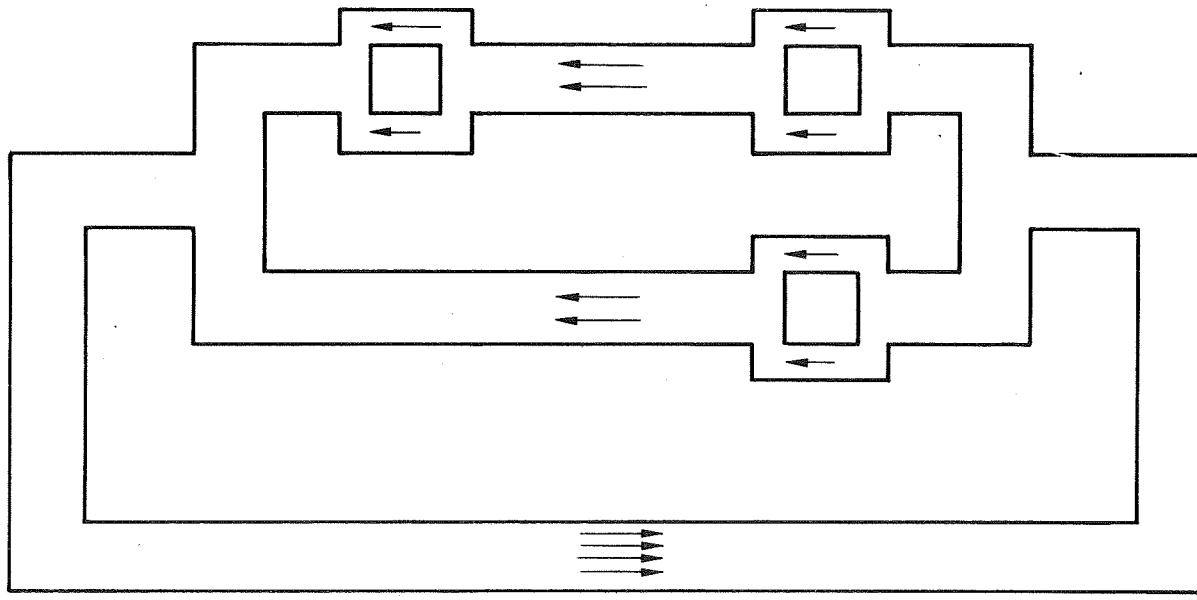
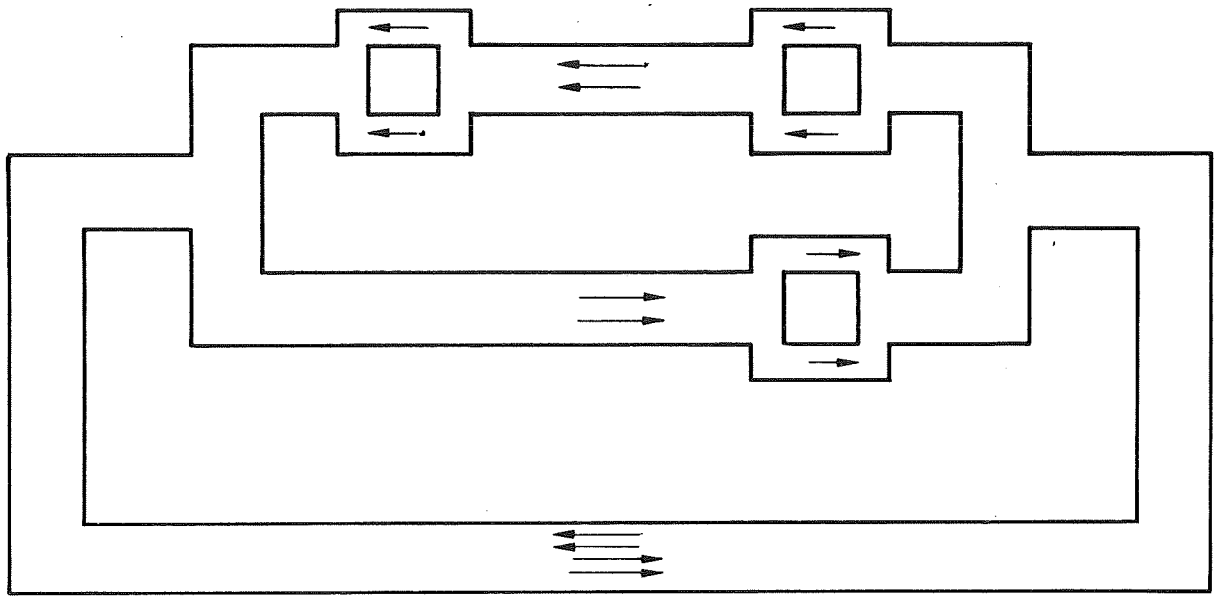


Fig. 11 Single-Stage Structure with Magnetic Path Identification



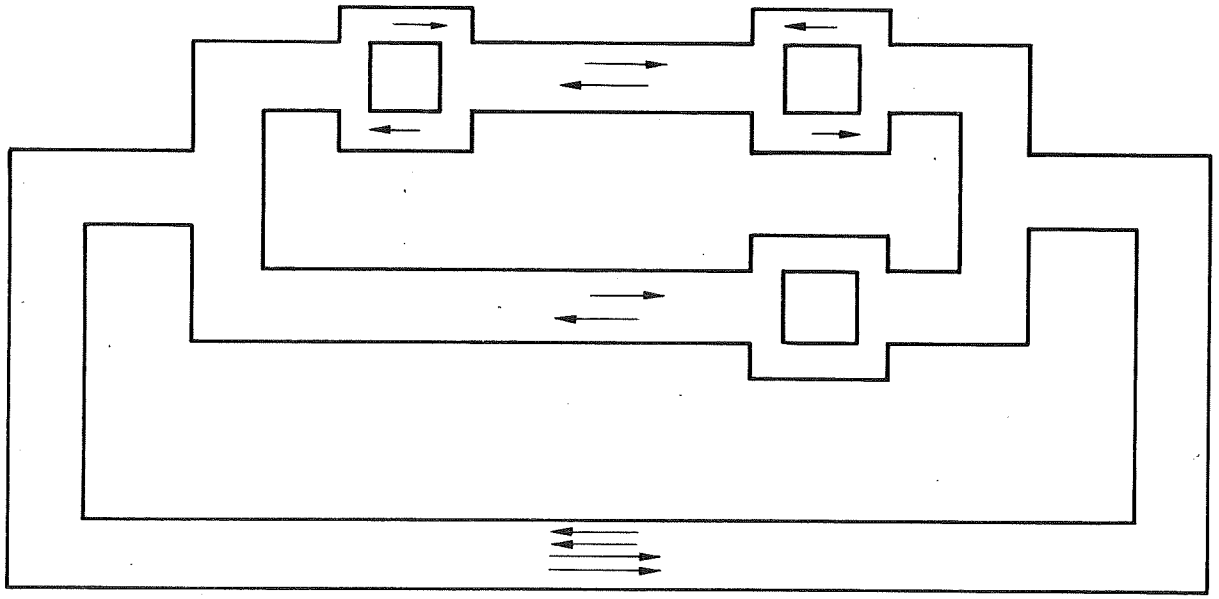
Clear State

Fig. 12a Flux States in the Single-Stage Structure



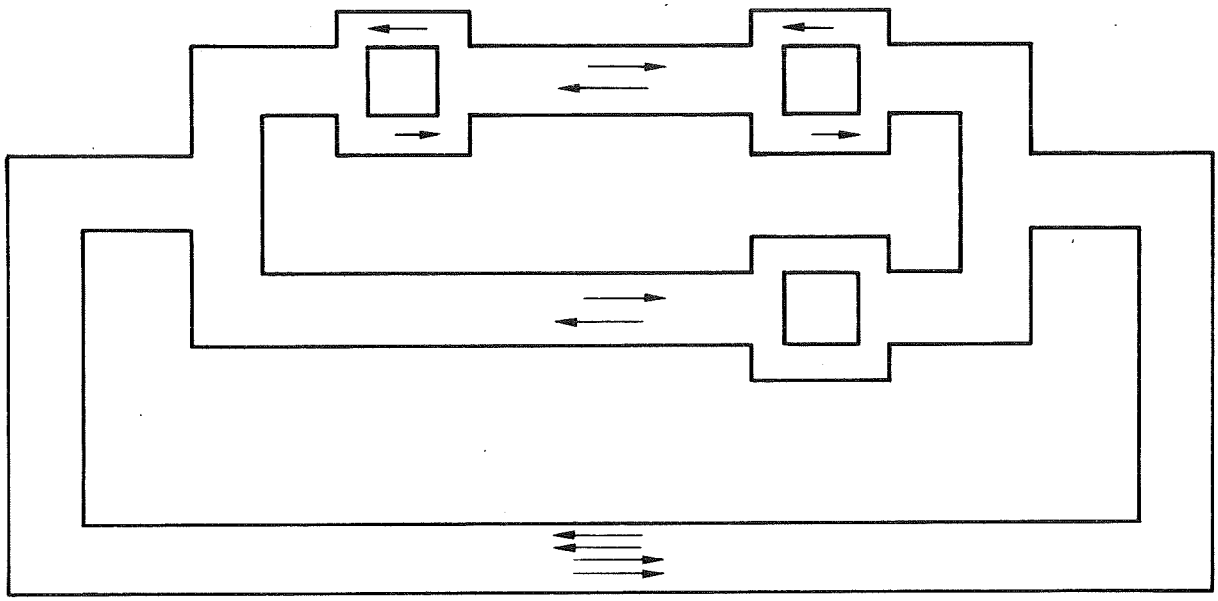
ZERO State

Fig. 12b Flux States in the Single-State Structure



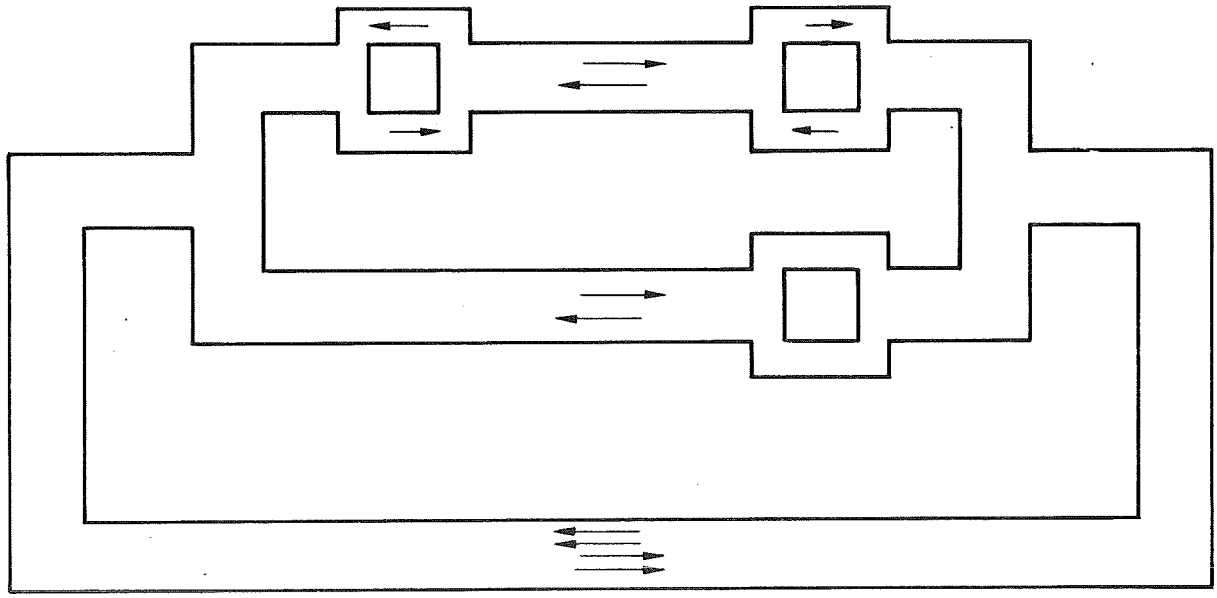
One State

Fig. 12c Flux States in the Single-Stage Structure



Decoupled ONE State

Fig. 12d Flux States in the Single-Stage Structure



Post One Transfer

Fig. 12e Flux States in the Single-Stage Structure

of the return leg is switched around the main aperture. The bias in the clear direction on legs 1 and 2 of the input aperture inhibits any flux change in leg A, in the absence of an input signal. The flux change for a binary ZERO transfer which is the absence of an input signal therefore is completed through leg B. This is shown in Fig. 12b.

In the case of a binary ONE transfer, an input signal is present at advance time in the form of a current through the coupling loop which links leg 1 of the input aperture. This current overcomes the effect of the bias current on that leg and causes the flux change produced by the flux drive winding to be completed equally through legs A and B. The fact that the input coupling loop links only leg 1 of the input aperture limits the possible flux change in leg A to half the flux capacity of that leg. This ONE state is shown in Fig. 12c. At the third clock time the transmitting stage, ie, the stage from which the input signal was derived, is reset to the clear state. This action causes a reverse current to flow in the coupling loop where a ONE had been transferred at the preceding advance time. The input aperture is unblocked* at this time and flux is switched around the input aperture by this reverse current. This produces the decoupled ONE state shown in Fig. 12d. At the fourth clock time the odd-to-even advance-pulse drive is applied to the "figure eight" winding linking the output aperture. The resultant drive mmf is in a direction to set leg 1 and to clear leg 2. For values of mmf below the threshold** of the stage aperture, flux will not change in either leg 1 or leg 2 of the output aperture when a stage is in the ZERO state, since the output aperture is blocked.

* When both legs of an aperture are saturated in the same direction relative to the main aperture, the aperture is said to be blocked since the flux can not be reversed locally around the aperture. When the two legs are saturated in opposite directions, the flux can be reversed locally around the aperture. In this case the aperture is said to be unblocked.[2]

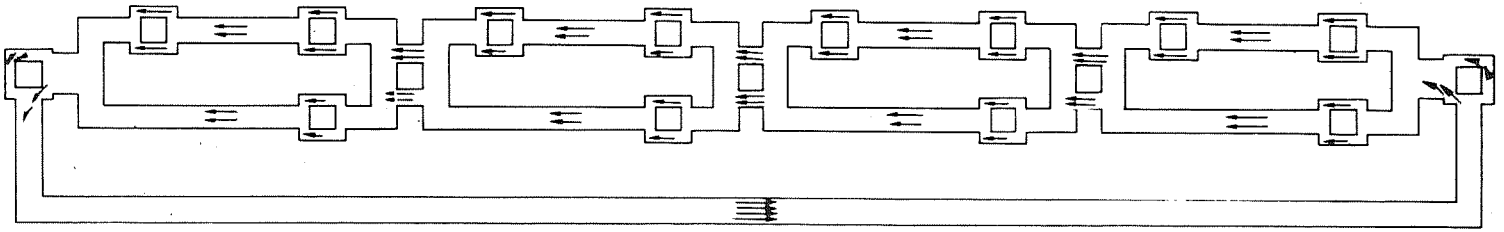
** The threshold is defined as that value of mmf (or the normalized equivalent, magnetic field strength H) which will irreversibly switch 5% of the flux capacity of the legs forming the magnetic path around an aperture.

When a stage is in a ONE state, the advance drive will produce a flux change in both legs around the output aperture as it is in an unblocked state. This flux change in turn induces a current in the coupling loop linking leg 1 of the output aperture. This post ONE transfer state is shown in Fig. 12e.

The operation of an integrated multistage structure is identical to the operation of a group of single-stage structures, except that the stages are joined together and they share a common return leg. The flux states showing the clear state and a 0100 pattern for the other three clock times are shown for the full-size structure in Figs. 13a through d. The flux states for the same pattern in the reduced size structure is shown in Figs. 14a through c.

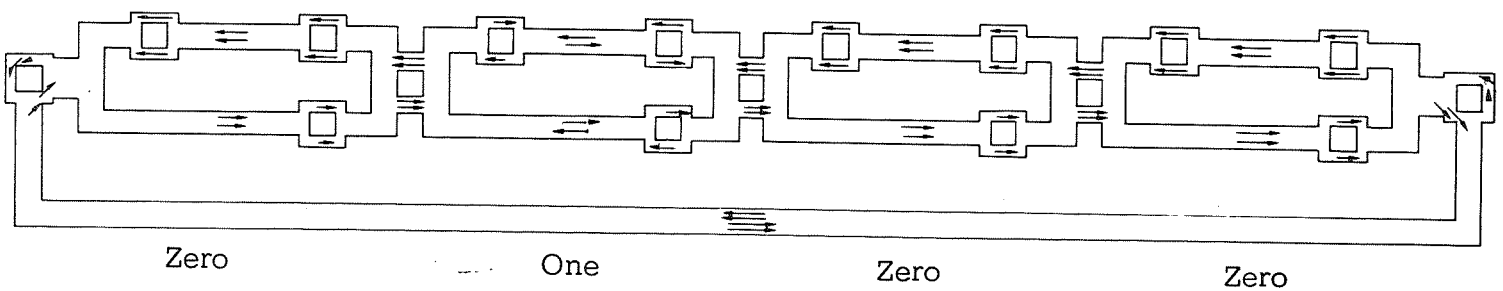
4.2.2 Importance of Partial Set State Thresholds

In the description of operation above it was stated that when the advance current applied to the output aperture was below the threshold of a stage, no switching would occur in leg 1 when a stage is in the ZERO state. When the advance current exceeds the stage threshold the noise signal out of all stages increases due to flux in leg 1 of the output aperture switching around the stage aperture. This causes a buildup of ZERO's to ONE's at a value only slightly above the stage threshold. For a stage in the ONE state the threshold of the stage is again the upper bound on the advance current. For advance currents below the stage threshold the flux set into leg 2 of the output aperture switches through leg 1 around the output aperture producing an output signal into the coupling loop. When the advance current exceeds the stage threshold, part of the flux set into leg 2 of the output aperture is switched around the stage aperture, thereby reducing the ONE flux available to produce an output signal. In both cases the stage threshold is the limit on the advance current. The stage thresholds, however, are different for the ZERO state and the ONE state. In the ZERO state, ideally, leg A is in the clear state and leg B is in the set state. As



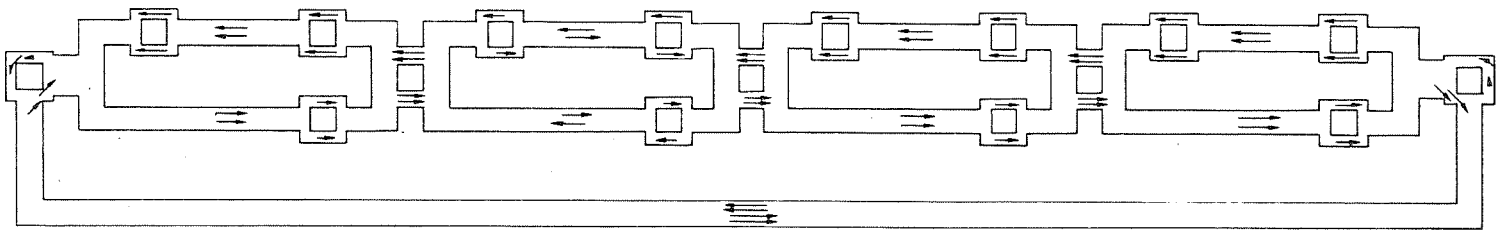
Clear State

Fig. 13a Flux States in the Full-Size Integrated Multistage Logic Structure



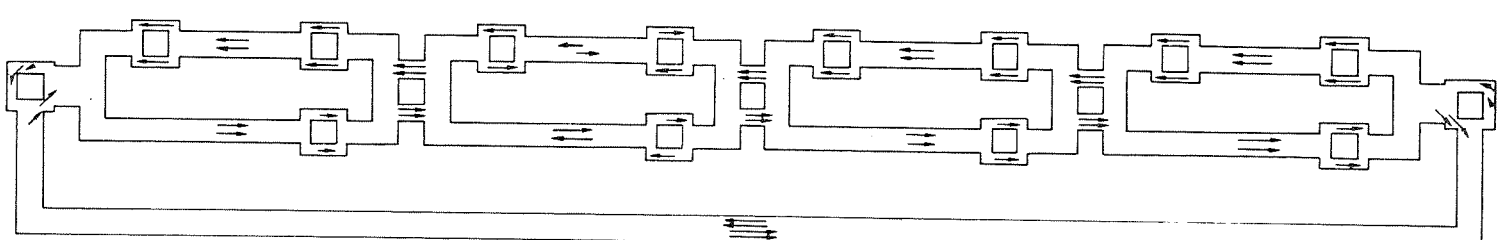
ZERO and ONE States

Fig. 13b Flux States in the Full-Size Integrated Multistage Logic Structure



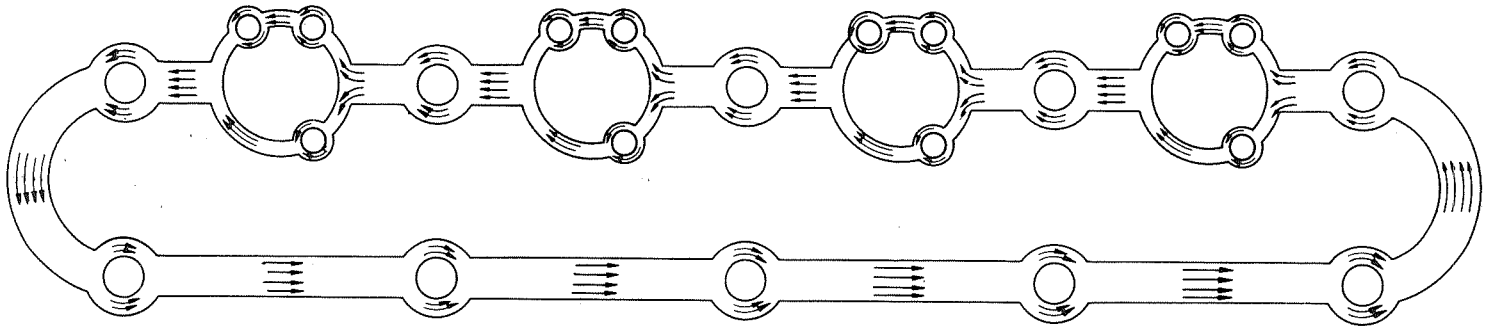
Decoupled ONE State

Fig. 13c Flux States in the Full-Size Integrated Multistage Logic Structure



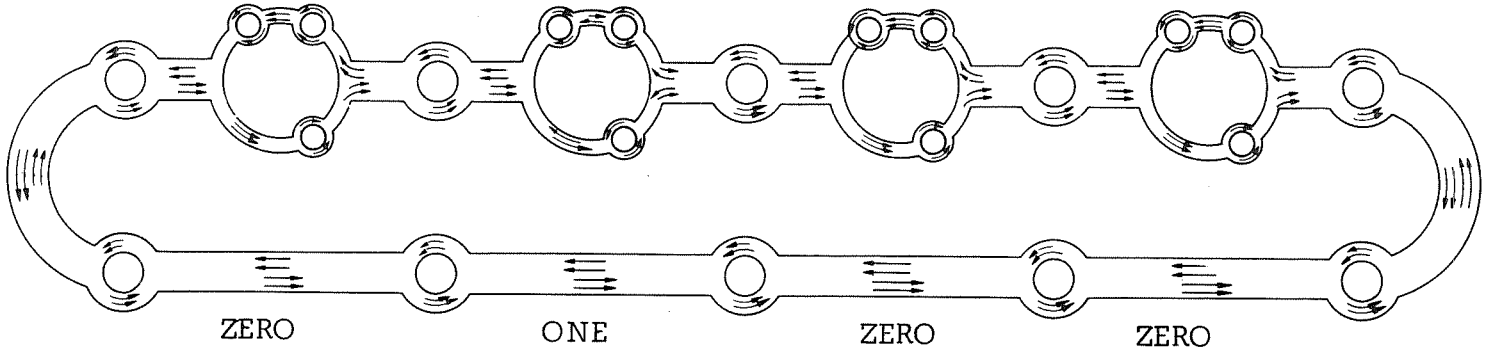
Post Transfer ONE State

Fig. 13d Flux States in the Full-Size Integrated Multistage Logic Structure



Clear State

Fig. 14a Flux States in the Reduced-Size Integrated Multistage Logic Structure



ZERO and ONE States

Fig. 14b Flux States in the Reduced-Size Integrated Multistage Logic Structure

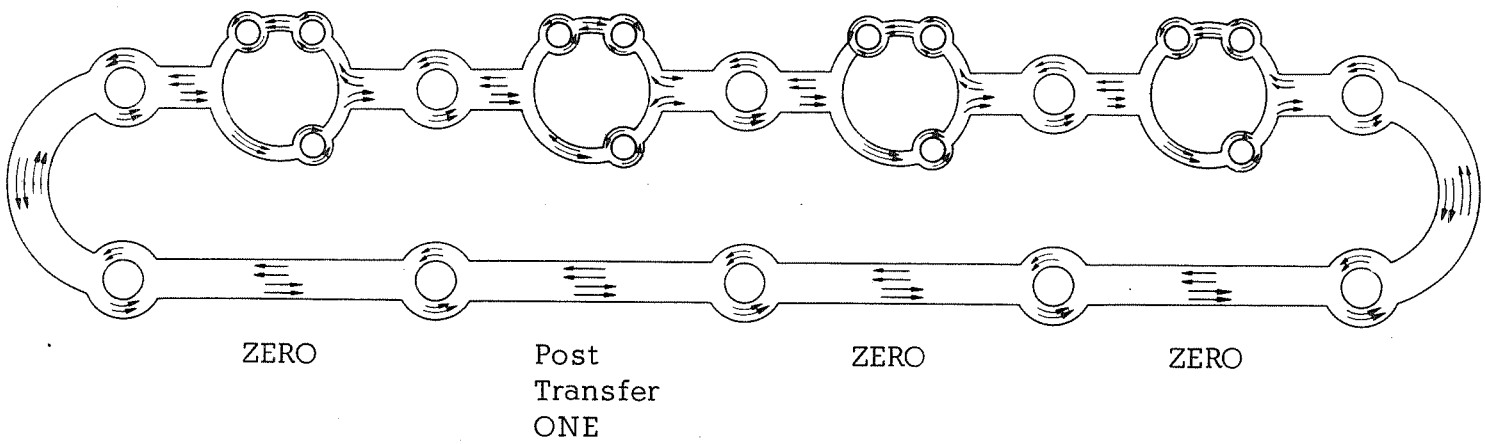


Fig. 14c Flux States in the Reduced-Size Integrated Multistage Logic Structure

the threshold is the same value for both of these states, the stage threshold is equal to the clear state threshold.

In the ONE state both leg A and leg B are 50% set. The stage threshold here depends upon the partial set state thresholds of the high H_c material. The partial set state thresholds for a typical square loop material are shown in Figs. 15 and 16. In Fig. 15 the relation of these thresholds to the B-H loop are shown. In Fig. 16 a profile shows the thresholds as a function of preset flux, given as a percentage of the flux capacity of the core. It is apparent that both the set direction threshold, TH_{ps}, and the clear direction threshold, TH_{pc}, are significantly lower than the clear state threshold. The stage threshold for the ONE state is the average of these two thresholds, as the magnetizing field in leg A due to the advance drive will be in the clear direction and in leg B the field will be in the set direction. For such a material the stage threshold for the ONE state would set the upper bound on advance current. This limit is about one third less than if the upper bound were determined by the ZERO state stage threshold.

The threshold characteristics of the high H_c material developed for the integrated structures are shown in Figs. 17 and 18. In Fig. 17 the thresholds relative to the B-H loop are shown. In Fig. 18 a profile for IS-25 material is shown. It is to be noted that the values of all of the partial set state thresholds have been raised relative to the clear state threshold and the average of the clear state and set state thresholds is greater than the clear state threshold. For this material, then, it is the ZERO state stage threshold that sets the upper bound on the advance current. For materials of comparable clear state threshold, the upper bound on advance current in structures made from material with enhanced thresholds is about 50% greater than in structures made from typical square loop

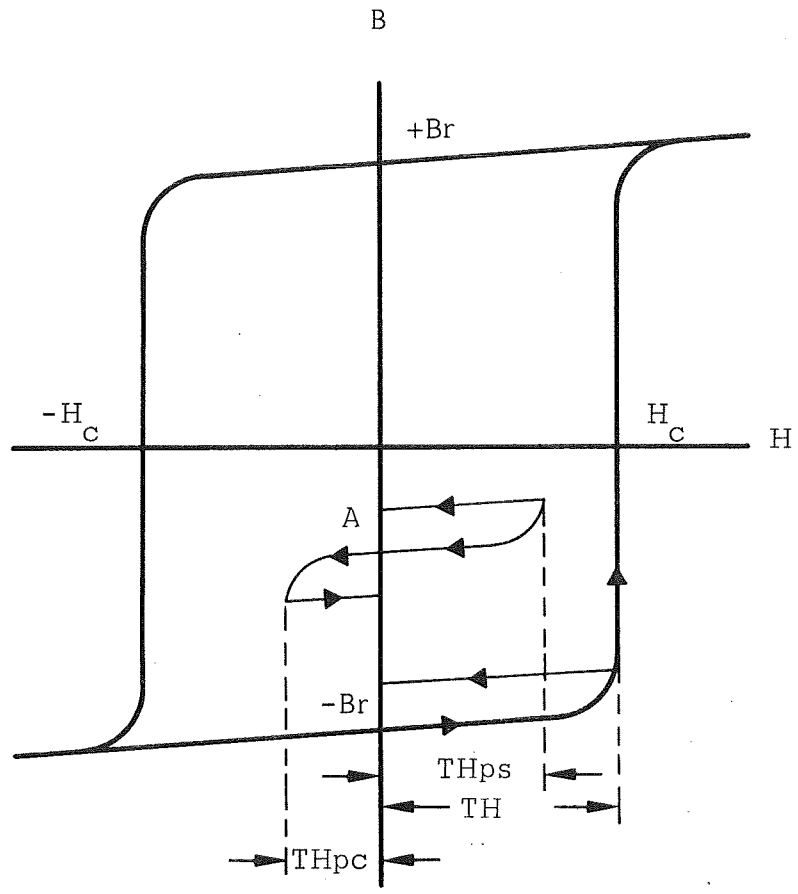


Fig. 15 Relation of Partial Set State Threshold to the B-H Loop of Typical Square Loop Materials Showing No Enhancement

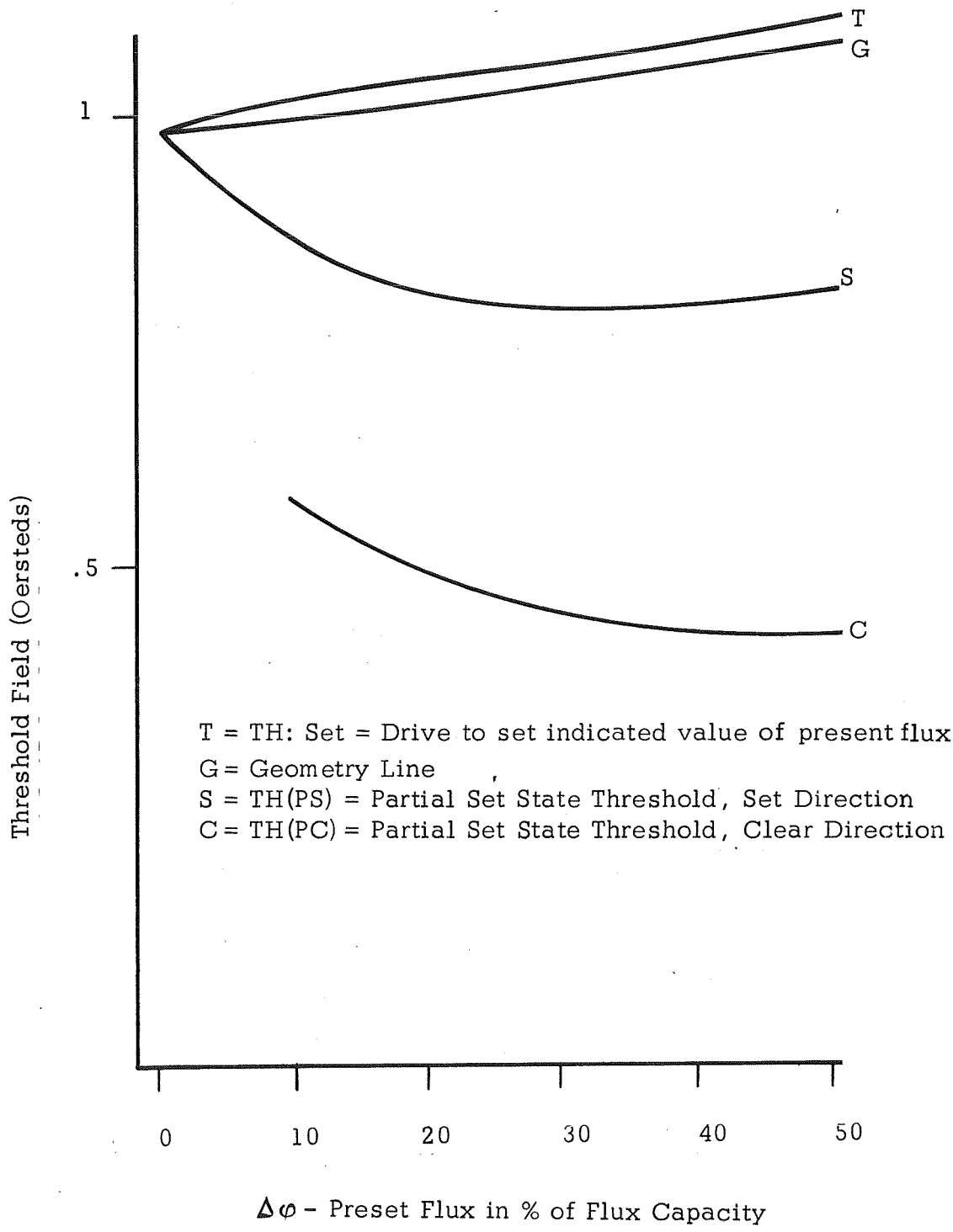


Fig. 16 Profile For Typical Square Loop Materials Showing No Enhancement

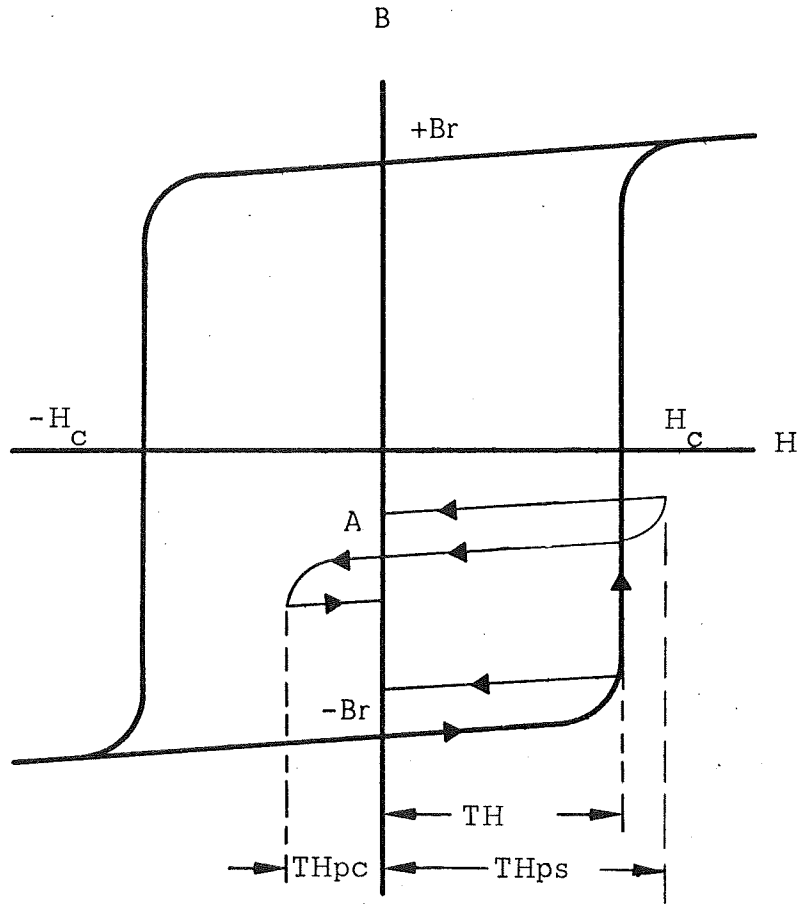
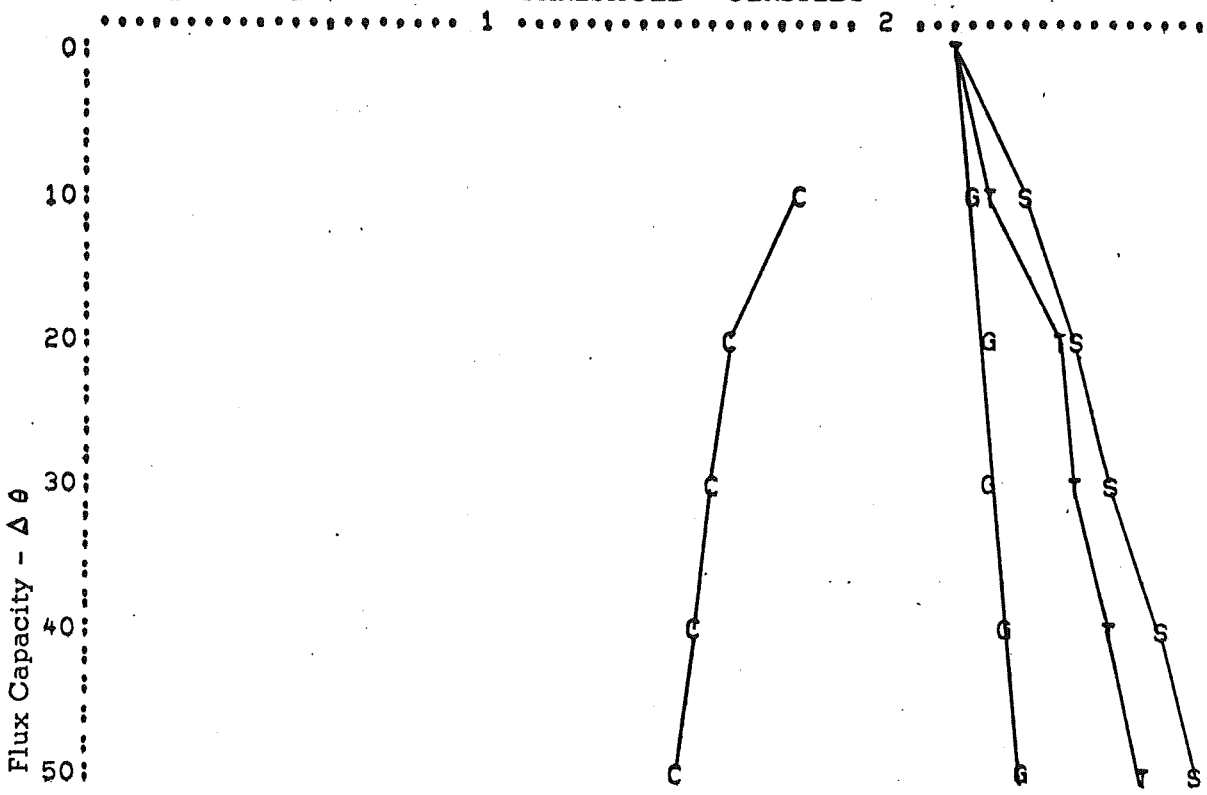


Fig. 17 Relation of Partial Set State Threshold to the B-H Loop For IS-25 Material

IS 25 349-1604 / 0.329 FIRING TEMP = 1300
CORE NUMBER 263 N2 TEMP = 1300

THE SCALE FOR THE ABSCISSA IS 2 PERCENT PER LINE.
THE SCALE FOR THE ORDINATE IS 0.043 OERSTEDS PER SPACE (1 OERSTED EQUALS 23 SPACES).



THE CORE DIAMETER IN INCHES IS 0.329
THE CORE MATERIAL IS IS 25-349
THE FIRING NUMBER IS 1604
THE CORE NUMBER IS 263
THE FIRING TEMP IS 1300
THE N2 TEMP IS 1300

TH = 2.121 OERSTEDS
TH(PS) = 2.734 OERSTEDS....FOR DEL. θ = 50 PERCENT
TH(PC) = 1.430 OERSTEDS....FOR DEL. θ = 50 PERCENT
TH(PS)/G(50) = 1.181
TH(PC)/G(50) = 0.618
TH(PC)/TH = 0.674

%.Δφ	TH:SET		TH(PS)		TH(PC)	
	OER.	A.T.	OER.	A.T.	OER.	A.T.
0	2.121	4.432				
10	2.200	4.596	2.307	4.820	1.746	3.648
20	2.380	4.972	2.432	5.080	1.551	3.240
30	2.435	5.088	2.504	5.232	1.539	3.216
40	2.531	5.288	2.633	5.500	1.478	3.088
50	2.621	5.476	2.734	5.712	1.430	2.988

Fig. 18 Profile Showing Partial Set State Thresholds as a Function of Preset Flux for IS-25 Material

materials.

4.2.3 Significance of Integrating High and Low H_c Materials

In the operation of all magnetic circuits there are two necessary conditions to be met: 1) The flux set into the receiver stage by the transfer of a logical ONE must be equal to or greater than the flux which had been set in the transmitter stage. 2) The flux set into the receiver stage by the transfer of a logical ZERO must be equal to or less than the flux which had been set in the transmitter stage. These conditions are shown graphically in the flux gain diagram of Fig. 19. To meet these conditions the available flux (the product of the flux change and turns) from the transmitter for a ONE must exceed the flux set into a receiver by the amount of the losses associated with the coupling loop and for a ZERO the coupling loop losses must exceed the available flux. This requirement has been reported in detail elsewhere.[3] This condition is generally accomplished by making the number of turns linking the transmitter to the coupling loop greater than those connecting the receiver to the coupling loop, ie, by means of a turns ratio. In addition, the current induced in the coupling loop for a ONE transfer must be of sufficient amplitude to switch or steer the flux in the receiver stage. In a circuit where the losses have been adequately provided for, the lower limit of the operating range for advance current is determined by the value which yields the minimum required coupling loop current. The upper bound, as discussed before, is determined by the thresholds of the transmitter stage. It is apparent that the upper bound can be raised by increasing the thresholds of the stage. This can be done either by increasing the path length of the stage or by increasing the coercive force. Generally it is desirable to reduce the path length of a stage, so this leaves increasing the coercive force as the only design variable. This method, however, would also raise the lower end of the range. By combining two materials and making the output aperture of a low H_c material, the lower end of the range can be held fixed.

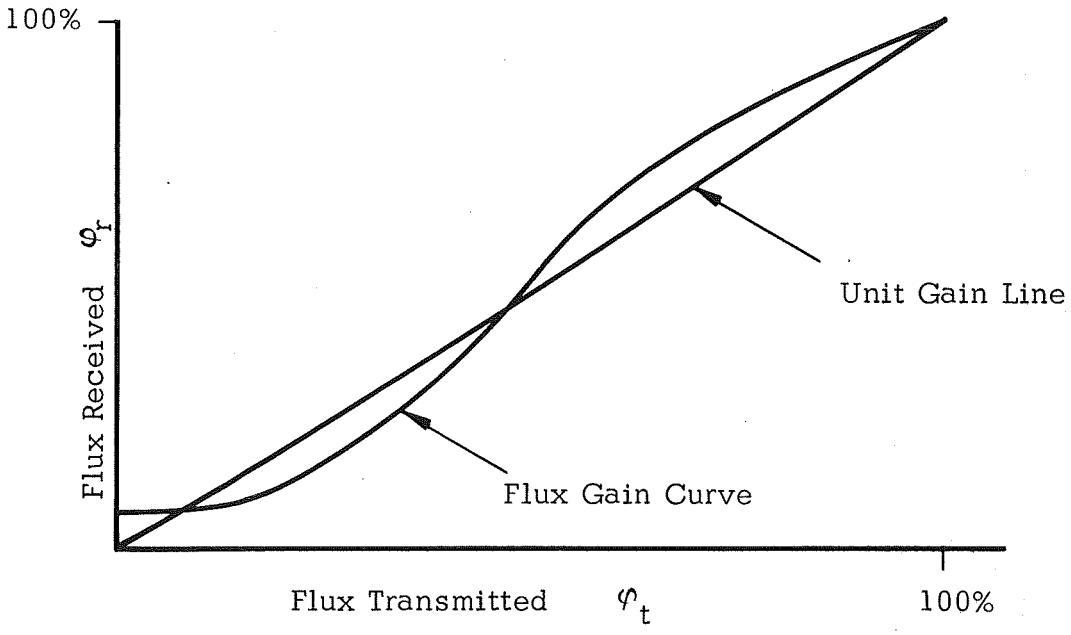


Fig. 19 Flux Gain Curve for Stable Operation

The effect on the advance current range due to a variation in the coercive force and due to use of bimaterial structures is shown in more detail in Fig. 20. In this figure the upper limit is taken as the threshold of the transmitter. The threshold of the output aperture is designated I_o in the figure for the case where the complete structure is made from the high H_c material and I_{ot} for the case where the output aperture is of a low H_c material. The line A shows the relation between coupling loop current, I_{cl}, and transfer switching time, t_s. It also shows the relation between advance current, I_t, and coupling loop current, for a hypothetical output aperture having no threshold and an infinitesmal switching characteristic. The effect of the threshold is to displace this line to the right, reducing the coupling loop current by the amount of the threshold. This displaced line is shown as line B. In addition the coupling loop current is reduced by the mmf, I_s, required to switch the output aperture at the transfer switching time, t_s, and is given by

$$I_s = \frac{G_{wt}}{t_s} \qquad (1)$$

where the switching constant of the transmitter, G_{wt}, is in ampere turn-microseconds. The transfer switching time is a function of the coupling loop current and the receiver stage switching constant, G_{wr}, and is given by

$$t_s = \frac{G_{wr}}{I_{cl}} \qquad (2)$$

Substituting (2) into (1) we obtain

$$I_s = \frac{G_{wt}}{G_{wr}} \; I_{cl} \qquad (3)$$

This curve is plotted in Fig. 20a for the full-size structure as line C. The lower limit of the range is obtained by finding the coupling loop current which will give a transfer switching time of 3 microseconds. This is the width of the drive pulses which sets the maximum transfer time. The advance current for this condition is found from the coupling

loop current and line C, thus arriving at the lower limit of the range for a bimaterial structure. The lower limit for a single-material structure of the high coercive force material is determined by the coupling loop current for a 3 microsecond transfer time and line D in Fig. 20a. Line D is shifted to the right of line C by an amount equal to the increase in the threshold of the output aperture. Had the low coercive force material been selected, the lower limit would have been given by line C, but now the upper end of the range would have been halved.

In Fig. 20b the determination of the range for the reduced-size structure is given. Since the path length around the stage aperture is reduced, the switching constant G_{wr} is also decreased, causing the transfer time to be reduced for a given value of coupling loop current. This is shown as an increased slope in line C. The lower limit of the range is found using line C and 3 microsecond transfer time. The low end of the range is seen to be lowered still further than the decrease obtained for two materials in a full-size structure shown in Fig. 20a. The low end of the range is thus seen to be reduced through the use of two materials in the integrated structures while the upper end of the range is held fixed. The range for a single-material reduced-size structure is also shown in Fig. 20b. Line D is drawn to reflect the higher threshold of the output aperture. The lower limit of the range is determined from the coupling loop current for 3 microsecond transfer time and line D. The improvement in range through the use of two materials is found by comparing the range for a single-material reduced-size structure with that for a two-material reduced-size structure.

4.2.4 Practical Considerations

The first attempts at operation of shift registers and ring counters were unsuccessful, even though the profile characteristics were as desired. Unity gain transfer was obtained for only a very few isolated transfers because of excessive leakage flux, ie, flux lines which pass through a surface of the structure and complete their path through the air. This

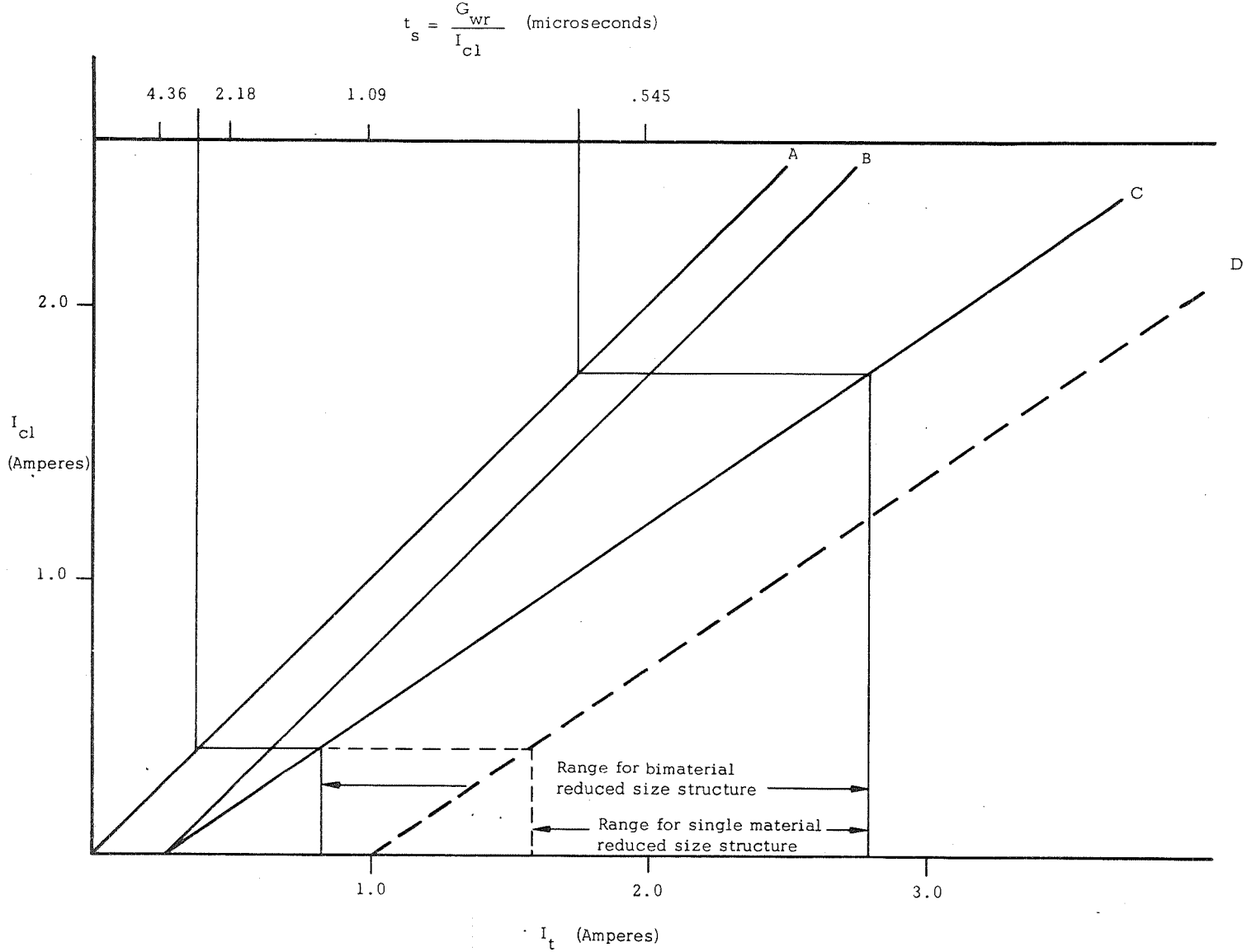


Fig. 20a Graphical Determination of Operating Range

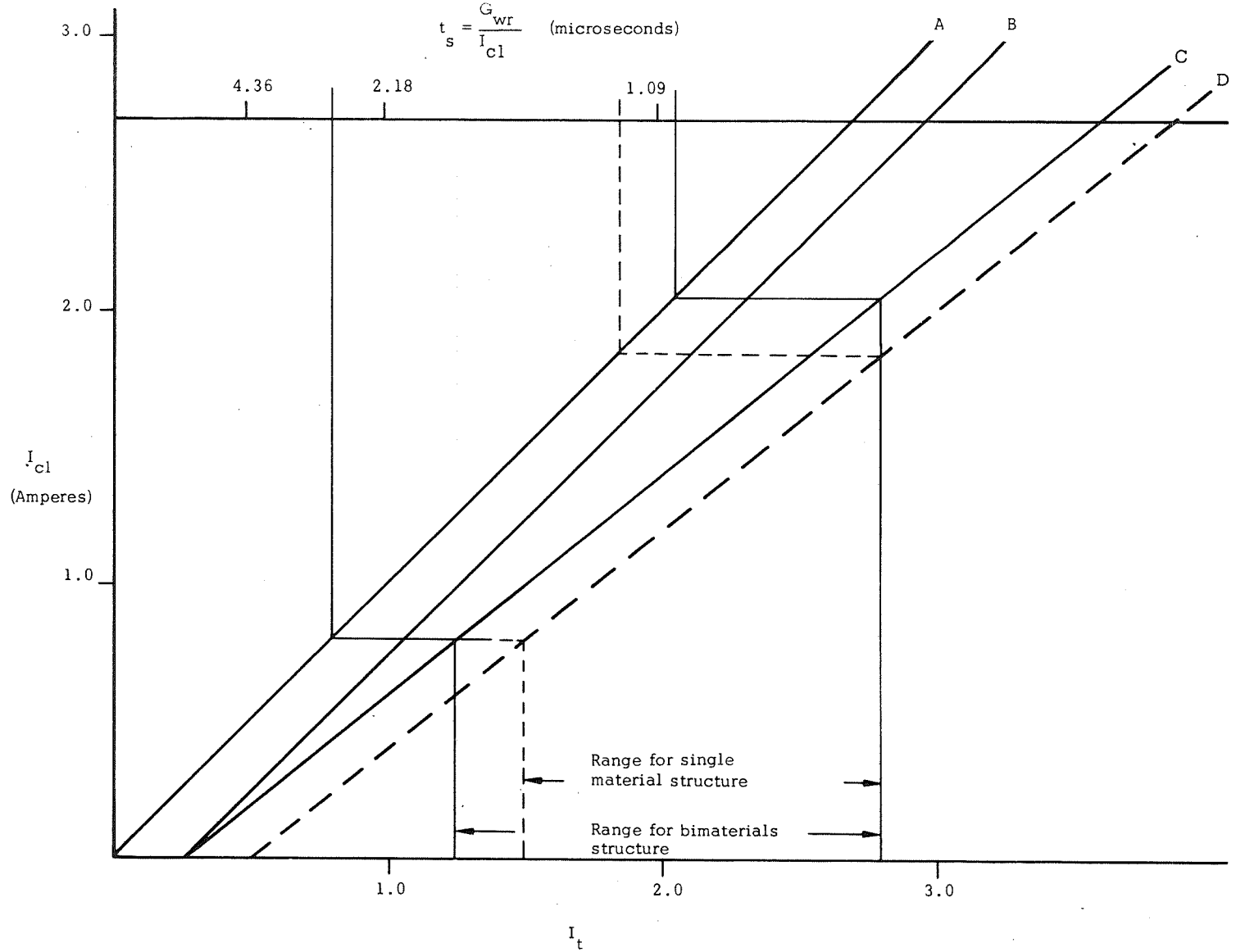


Fig. 20b Graphical Determination of Operating Range

problem is aggravated for structures of high surface-to-volume ratio and materials of high coercive force.

Simple experiments at reducing the leakage flux with eddy current shields gave a small reduction in the leakage flux but as the structures were wound, the copper shields could not be brought close enough to the surface to be very effective. The process developed for plating conductor patterns on the structures* was utilized to plate eddy current shields on three of their four sides. These structures when wired for shift register and ring counter operation worked with a minimum of preliminary adjustments. The eddy current shields were used on structures for both the full-size and the reduced-size registers. The eddy current shields are 0.004" thick plated copper. A problem encountered with the eddy current shield was one of short circuits between the conductors around the structures and the eddy current shield. This problem was eliminated by coating the structures with an insulating layer of Pyre ML.**

The major problem due to leakage flux arose around the output aperture when driven at advance time. Leg 1 of the output aperture when driven in the set direction for a ZERO transfer ideally cannot switch for values of advance current below the threshold of the stage. A significant flux change in leg 1 did in fact occur, passing through the surface of leg A on one side of the aperture and impinging on the surface of leg A on the other side of the output aperture, completing a path through the air. The effect of this leakage flux was to give an excessively large noise signal. The plated-on eddy current shield described above has greatly reduced the leakage flux and thereby the noise signal. Leakage flux has not been fully eliminated, however, as the shield covers only three of the four surfaces.

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* See Section 5.0 - Plated Conductors

** A high temperature insulating varnish by E.I. DuPont with very good resistance to environmental damage.

4.3 Test Results of Structures

During this program a number of structures were prepared by different processes using different binder compositions and proportions. The structures selected for final temperature tests were all prepared from punching or molding blanks thermopressed from powder.

The tests conducted on each structure consisted of taking a profile of the stage aperture and one of the output aperture for selected stages at specified temperatures. At room temperature, profiles of all stages were taken. At -20°C, 0°C, +60°C (for the full-size structures only) and at +100°C profiles for the first and third stages only were taken. The tests were taken on two test jigs supplied by Langley Research Center. The structures fitted over a set of pins and the test windings were completed by closing the jig. These jigs with structures on the pins are shown in Figs. 21 and 22. Two of the full-size structures have had eddy current shields plated on them prior to testing.

Test data summarizing the threshold characteristics for stage 1 of each structure for all temperatures are given in Tables 5 and 6. The identification of each sample with regard to material, firing number, and core number is given in Appendix I.

4.4 Test Results of Registers

4.4.1 Windings

The windings used for the registers wired from full-size structures and the registers wired from the reduced-size structures are listed in Tables 7 and 8 respectively. The positioning of the windings for the reduced size registers are shown in Fig. 23. The windings used on the full size registers differed slightly in placement from that shown but produced equivalent flux states. The only winding in which the wire size was found to be critical for operation is the coupling loop. For the coupling loops two #33 size wires were used for full-size registers and one #30 size wire for the reduced-size

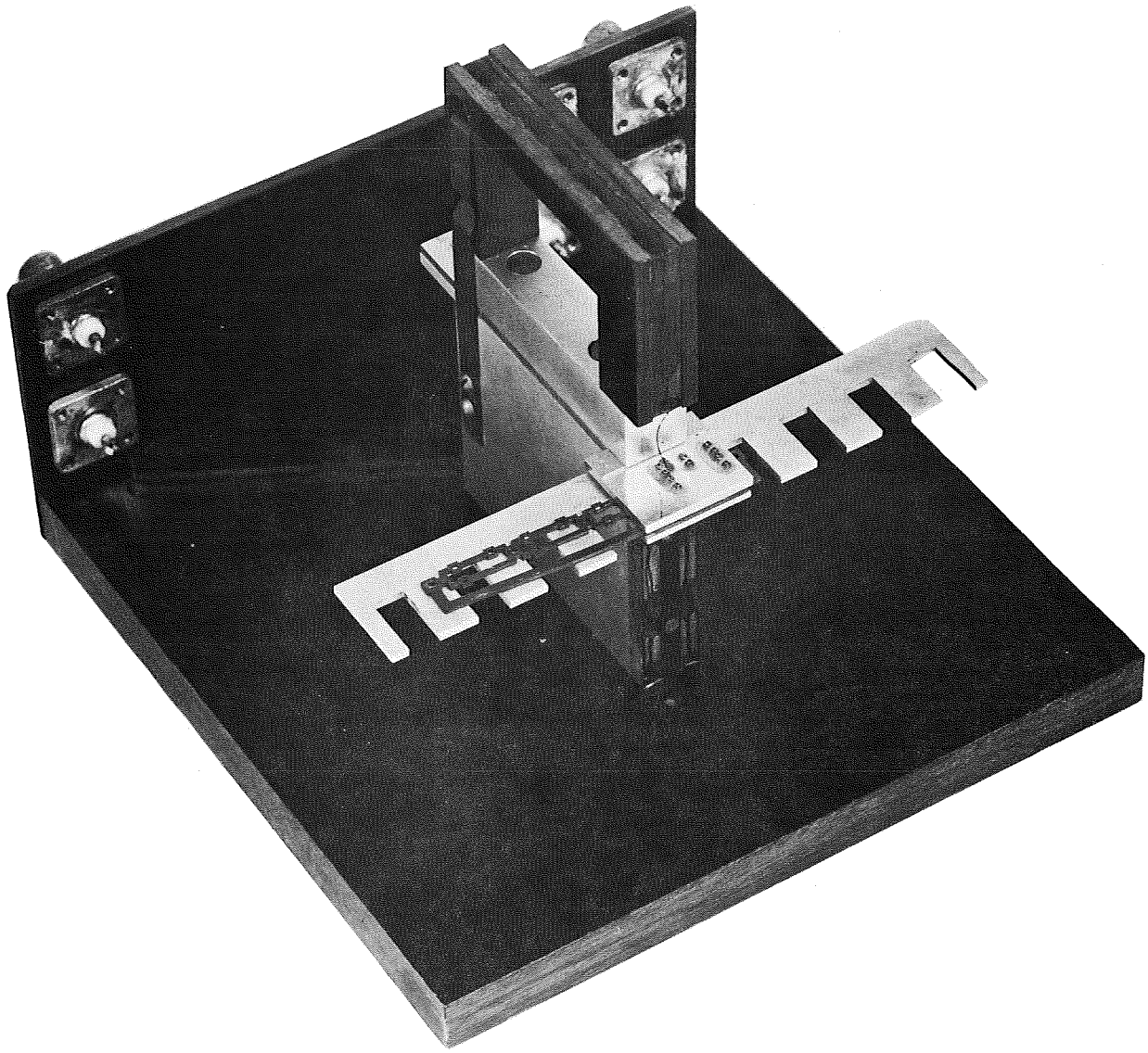


Fig. 21 Test Jig for Full-Size Structures

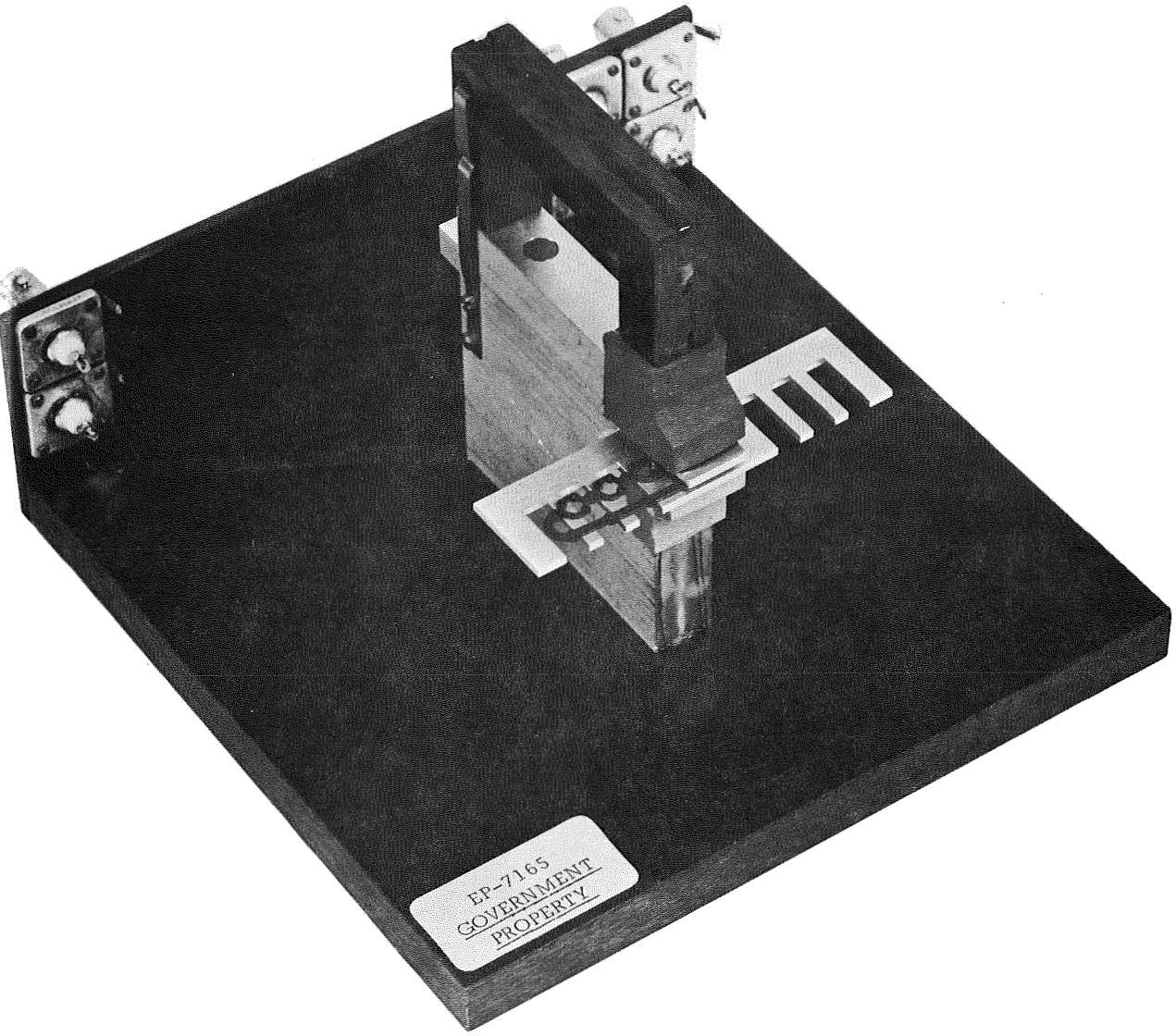


Fig. 22 Test Jig for Reduced-Size Structures

Specimen	Aperture*	Parameter	Temperature (°C) -20	0	+20/Rm Temp	+60	+100
F1	Stage	TH	2.7	2.4	2.2	1.8	1.3
"	"	TH_{ps}	3.4	3.2	2.7	2.2	1.7
"	"	TH_{pc}	1.7	1.7	1.4	1.2	0.7
"	Output	TH	0.8	0.7	0.7	0.6	0.5
"	"	TH_{ps}	1.4	1.1	0.84	0.6	0.4
"	"	TH_{pc}	0.5	0.5	0.4	0.3	0.1
F2	Stage	TH	2.8	2.5	2.3	1.9	1.3
"	"	TH_{ps}	3.5	3.2	2.8	2.3	1.8
"	"	TH_{pc}	1.8	1.7	1.4	1.2	0.8
"	Output	TH	0.7	0.7	0.6	0.6	0.4
"	"	TH_{ps}	1.4	1.1	0.9	0.6	0.3
"	"	TH_{pc}	0.5	0.5	0.4	0.2	0.1
F3	Stage	TH	2.8	2.5	2.3	1.9	1.3
"	"	TH_{ps}	3.6	3.2	2.9	2.4	1.8
"	"	TH_{pc}	1.7	1.7	1.4	1.2	0.8
"	Output	TH	0.8	0.7	0.7	0.6	0.5
"	"	TH_{ps}	1.4	1.1	0.9	0.6	0.4
"	"	TH_{pc}	0.5	0.5	0.4	0.3	0.1
F4	Stage	TH	2.7	2.4	2.2	1.8	1.3
"	"	TH_{ps}	3.5	3.2	2.8	2.3	1.8
"	"	TH_{pc}	1.8	1.7	1.4	1.2	0.8
"	Output	TH	0.8	0.7	0.7	0.6	0.5
"	"	TH_{ps}	1.4	1.1	0.9	0.6	0.3
"	"	TH_{pc}	0.5	0.5	0.4	0.3	0.1
F5	Stage	TH	2.3	2.2	2.0	1.5	1.0
"	"	TH_{ps}	3.4	3.1	2.7	2.2	1.7
"	"	TH_{pc}	1.7	1.6	1.4	1.0	0.7
"	Output	TH	0.7	0.7	0.7	0.6	0.5
"	"	TH_{ps}	1.3	1.1	0.9	0.6	0.3
"	"	TH_{pc}	0.5	0.5	0.4	0.3	0.1
F6	Stage	TH	2.5	2.3	2.1	1.6	1.1
"	"	TH_{ps}	3.4	3.0	2.7	2.2	1.6
"	"	TH_{pc}	1.8	1.6	1.4	1.0	0.7
"	Output	TH	0.7	0.7	0.6	0.5	0.4
"	"	TH_{ps}	1.3	1.1	0.8	0.5	0.3
"	"	TH_{pc}	0.5	0.4	0.4	0.2	0.1
F7	Stage	TH	3.0	2.8	2.6	2.1	1.4
"	"	TH_{ps}	3.7	3.4	3.1	2.5	2.0
"	"	TH_{pc}	2.0	1.9	1.7	1.3	0.8
"	Output	TH	0.7	0.8	0.8	0.8	0.6
"	"	TH_{ps}	2.0	1.8	1.4	1.0	0.7
"	"	TH_{pc}	0.7	0.6	0.6	0.5	0.3
F8	Stage	TH	2.6	2.5	2.1	1.8	1.4
"	"	TH_{ps}	3.2	3.0	2.8	2.2	1.8
"	"	TH_{pc}	1.8	1.6	1.2	1.2	0.9
"	Output	TH	1.0	0.9	0.8	0.7	0.6
"	"	TH_{ps}	2.6	2.3	2.0	1.6	1.2
"	"	TH_{pc}	1.0	0.9	0.8	0.7	0.5
F9	Stage	TH	2.6	2.5	2.2	1.9	1.3
"	"	TH_{ps}	3.2	3.0	2.7	2.3	1.7
"	"	TH_{pc}	1.7	1.6	1.4	1.1	0.8
"	Output	TH	1.3	1.3	1.1	1.0	0.7
"	"	TH_{ps}	1.9	1.7	1.4	1.1	0.8
"	"	TH_{pc}	1.2	0.9	0.8	0.6	0.4
F10	Stage	TH	2.6	2.4	2.1	1.7	1.1
"	"	TH_{ps}	3.4	3.1	2.8	2.2	1.7
F10	Stage	TH_{pc}	1.8	1.7	1.4	1.0	0.7
"	Output	TH	0.6	0.6	0.6	0.5	0.4
"	"	TH_{ps}	1.5	1.2	0.9	0.6	0.5
"	"	TH_{pc}	0.5	0.4	0.5	0.3	0.2

* All data for Stage 1 of each structure.

Table 6 Threshold vs Temperature: Reduced-Size Integrated Logic Structures

Specimen	Aperture*	Parameter	Temperature (°C) -20	0	+20/R.T.	+100
R1	Stage	TH	3.6	3.3	2.9	1.9
"	"	TH_{ps}	6.1	5.5	5.0	3.2
"	"	TH_{pc}	2.5	2.1	1.9	1.1
"	Output	TH	2.0	1.8	1.6	1.1
"	"	TH_{ps}	4.2	3.8	3.3	2.1
"	"	TH_{pc}	1.6	1.5	1.3	0.8
R2	Stage	TH	3.4	3.2	2.8	1.7
"	"	TH_{ps}	5.9	5.5	4.9	3.1
"	"	TH_{pc}	2.3	2.1	1.8	1.1
"	Output	TH	1.4	1.2	1.1	0.7
"	"	TH_{ps}	4.1	3.8	3.3	2.0
"	"	TH_{pc}	1.5	1.3	1.2	0.6
R3	Stage	TH	3.4	3.2	2.9	1.8
"	"	TH_{ps}	6.5	5.6	5.1	3.3
"	"	TH_{pc}	2.0	2.0	1.9	1.0
"	Output	TH	1.8	1.8	1.6	1.0
"	"	TH_{ps}	4.3	4.0	3.3	2.2
"	"	TH_{pc}	1.7	1.6	1.4	0.9
R4	Stage	TH	3.6	3.2	2.9	1.8
"	"	TH_{ps}	6.2	5.7	5.0	3.2
"	"	TH_{pc}	2.3	1.9	1.9	1.2
"	Output	TH	1.3	1.2	1.1	0.7
"	"	TH_{ps}	1.4	1.4	1.1	0.4
"	"	TH_{pc}	0.9	0.7	0.6	0.2
R5	"	TH	3.9	3.9	3.2	2.3
"	"	TH_{ps}	7.0	7.7	6.2	4.3
"	"	TH_{pc}	2.6	2.1	1.8	1.2
"	Output	TH	1.1	1.1	0.8	0.5
"	"	TH_{ps}	2.7	2.7	2.1	1.3
"	"	TH_{pc}	1.3	1.2	0.9	0.6
R6	Stage	TH	4.0	3.5	3.4	2.3
"	"	TH_{ps}	7.4	6.8	6.3	4.1
"	"	TH_{pc}	2.4	2.0	1.9	1.2
"	Output	TH	1.8	1.6	1.4	1.0
"	"	TH_{ps}	2.6	2.3	2.1	1.2
"	"	TH_{pc}	1.5	1.3	1.2	0.6
R7	Stage	TH	3.9	3.7	3.3	2.2
"	"	TH_{ps}	7.0	6.2	5.6	3.7
"	"	TH_{pc}	2.6	2.2	1.9	1.2
"	Output	TH	1.9	1.7	1.5	1.0
"	"	TH_{ps}	2.4	2.1	1.8	1.0
"	"	TH_{pc}	1.5	1.3	1.0	0.6
R8	Stage	TH	3.6	3.3	2.9	1.9
"	"	TH_{ps}	7.2	6.5	5.7	3.8
"	"	TH_{pc}	2.5	2.1	1.8	1.1
"	Output	TH	1.7	1.7	1.4	1.0
"	"	TH_{ps}	3.2	2.8	2.5	1.5
"	"	TH_{pc}	1.6	1.3	1.3	0.7
R9	Stage	TH	3.6	3.2	2.9	1.9
"	"	TH_{ps}	6.7	6.0	5.4	3.5
"	"	TH_{pc}	2.4	2.1	1.9	1.3
"	Output	TH	1.7	1.5	1.4	1.0
"	"	TH_{ps}	2.9	2.5	2.0	1.0
"	"	TH_{pc}	1.3	1.0	1.0	0.5
R10	Stage	TH	3.8	3.4	3.1	2.0
"	"	TH_{ps}	8.5	7.5	7.1	4.7
"	"	TH_{pc}	2.0	1.7	1.6	1.0
"	Output	TH	1.5	1.3	1.2	0.8
"	"	TH_{ps}	3.1	2.6	2.4	1.5
"	"	TH_{pc}	1.7	1.5	1.2	0.8

*All data for Stage 1 of each structure

Table 7 Windings: Full-Size Registers

Drive apertures leg 1	1 turn/aperture	I2 bias
Return leg	20 turns/structure	Flux drive
" "	20 turns/ "	Clear
Stage	16 turns/"	Flux drive
Stage	16 turns/"	Clear
Input aperture:		
Leg 1	1 turn/stage	I1 bias
Leg 1	1 turn/"	Coupling loop
Leg 2	1 turn/"	I2 bias
Output aperture:	1 turn Figure 8/stage	Advance
Leg 1	1 turn/stage	Clear
Leg 1	2 turns/stage	Coupling loop
Leg 2	2 turns/ "	Clear
Clipper core	1 turn/ "	Set Clipper
" "	1 turn/ "	Clear Clipper
Sense leads:		
Leg A		
Leg B		
Input aperture leg 1		
Input aperture leg 2		
Output aperture leg 1	Per stage	
Output aperture leg 2		
Clipper cores		
Return leg per structure		

Table 8 Windings: Reduced-Size Registers

Drive aperture	1 turn Figure 8/aperture	Flux drive
Return leg	10 turns/structure	Clear
Stage	10 turns/ "	Clear
Input aperture leg 1	1 turn/stage	I1 bias
" " leg 1	1 turn/ "	Coupling loop
" " leg 2	1 turn/ "	I2 bias
Output aperture	1 turn Figure 8	Advance
" " leg 1	1 turn/stage	Clear
" " leg 1	2 turn/ "	Coupling loop
" " leg 2	2 turn/ "	Clear
Clipper core	1 turn/ "	Set Clipper
" "	1 turn/ "	Clear Clipper

Sense leads:

leg A

leg B

Input aperture leg 1
Input aperture leg 2
Output aperture leg 1
Output aperture leg 2
Clipper core
} per stage

Return leg per aperture

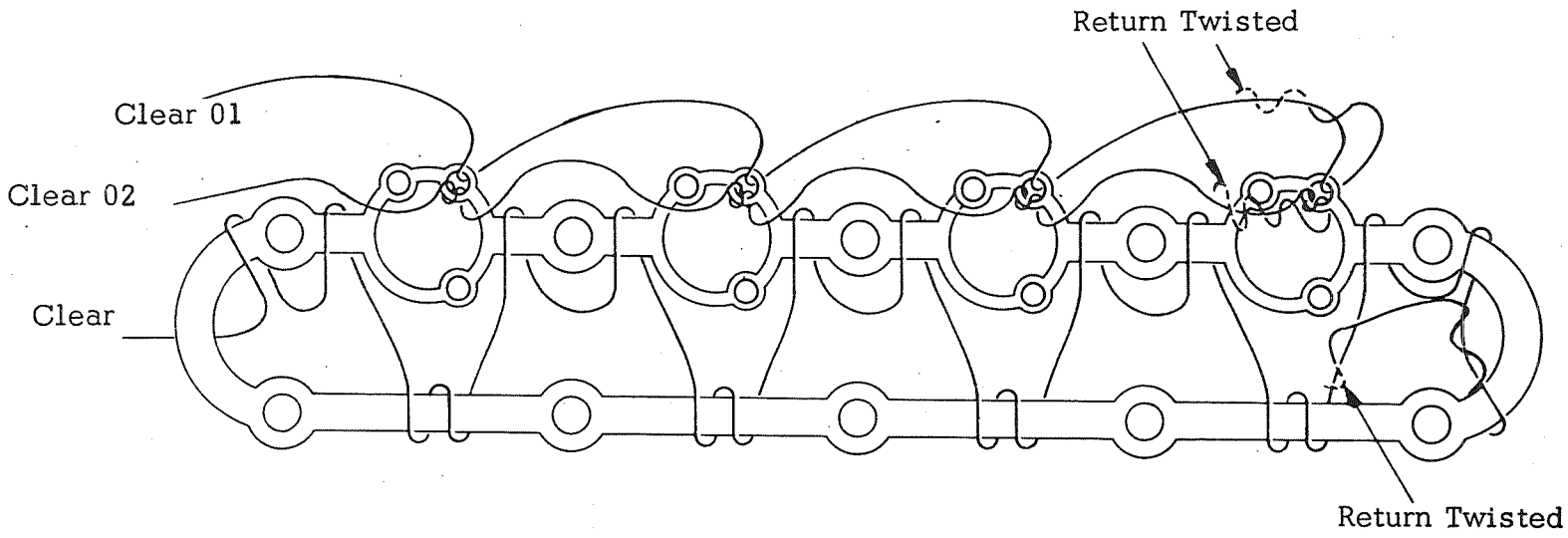


Fig. 23a Clear Windings

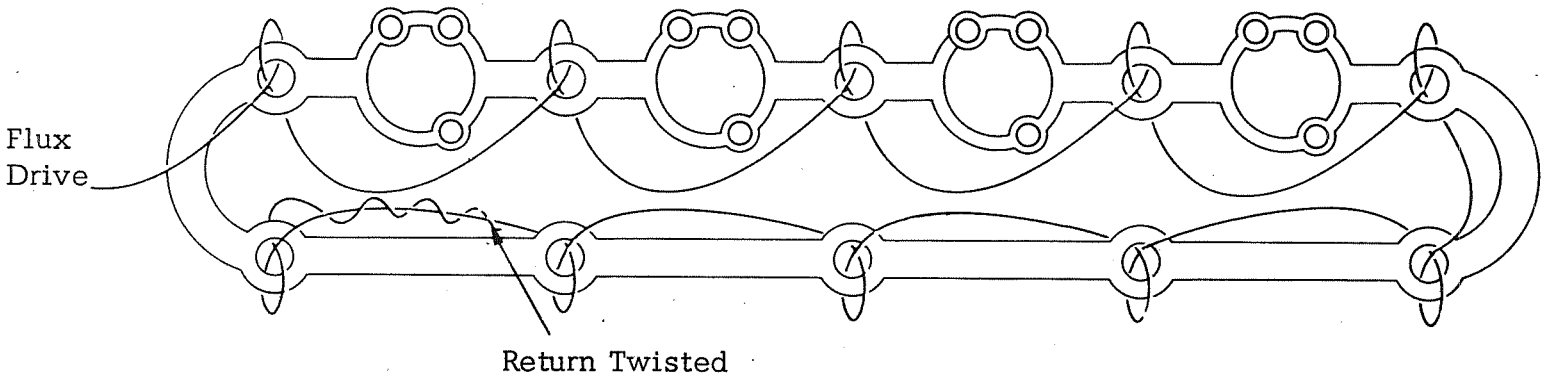


Fig. 23b Flux Drive Winding

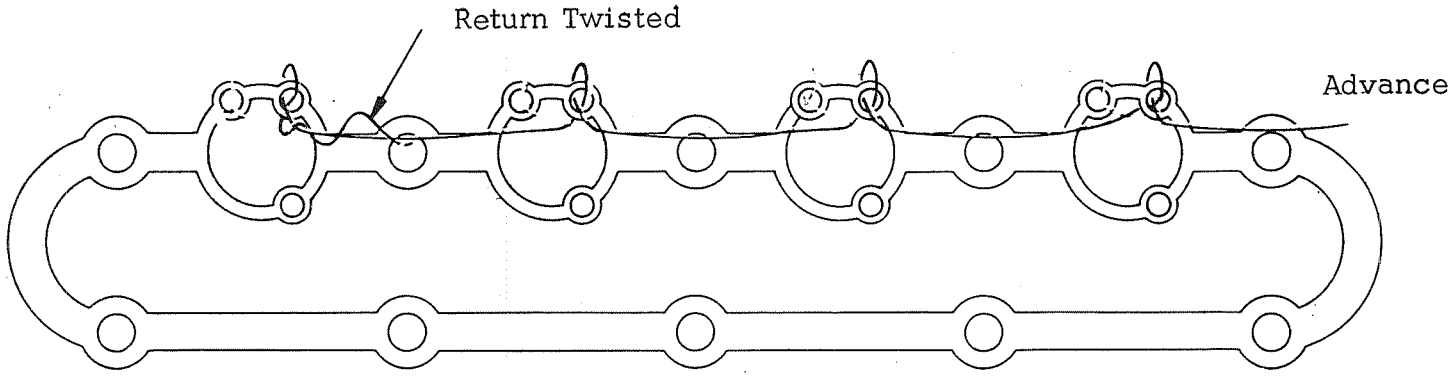


Fig. 23c Advance Windings

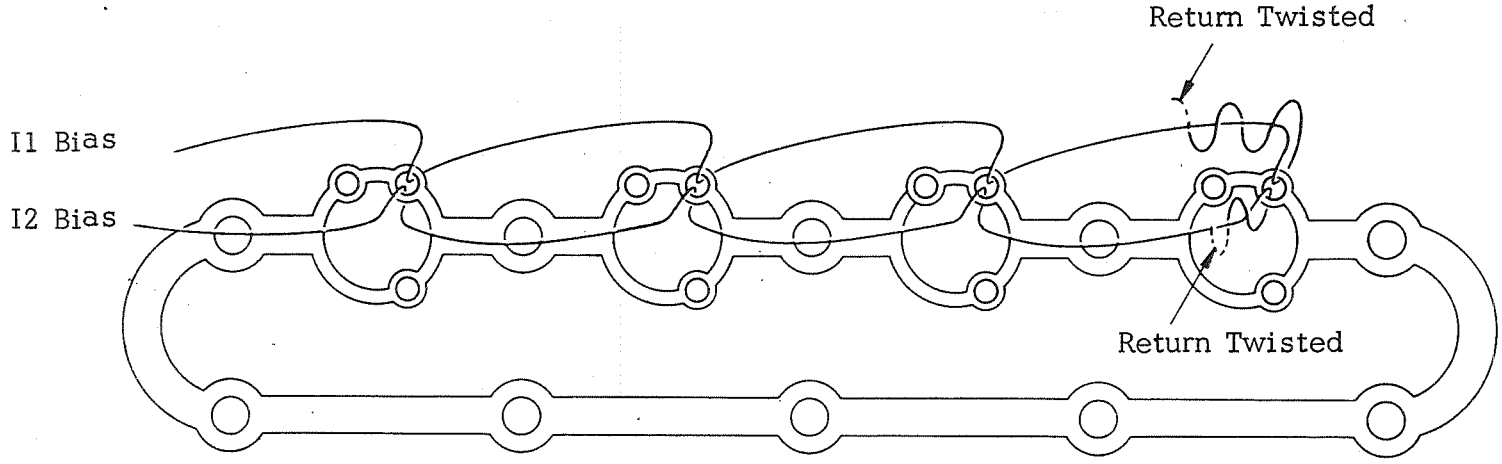


Fig. 23d Bias Windings

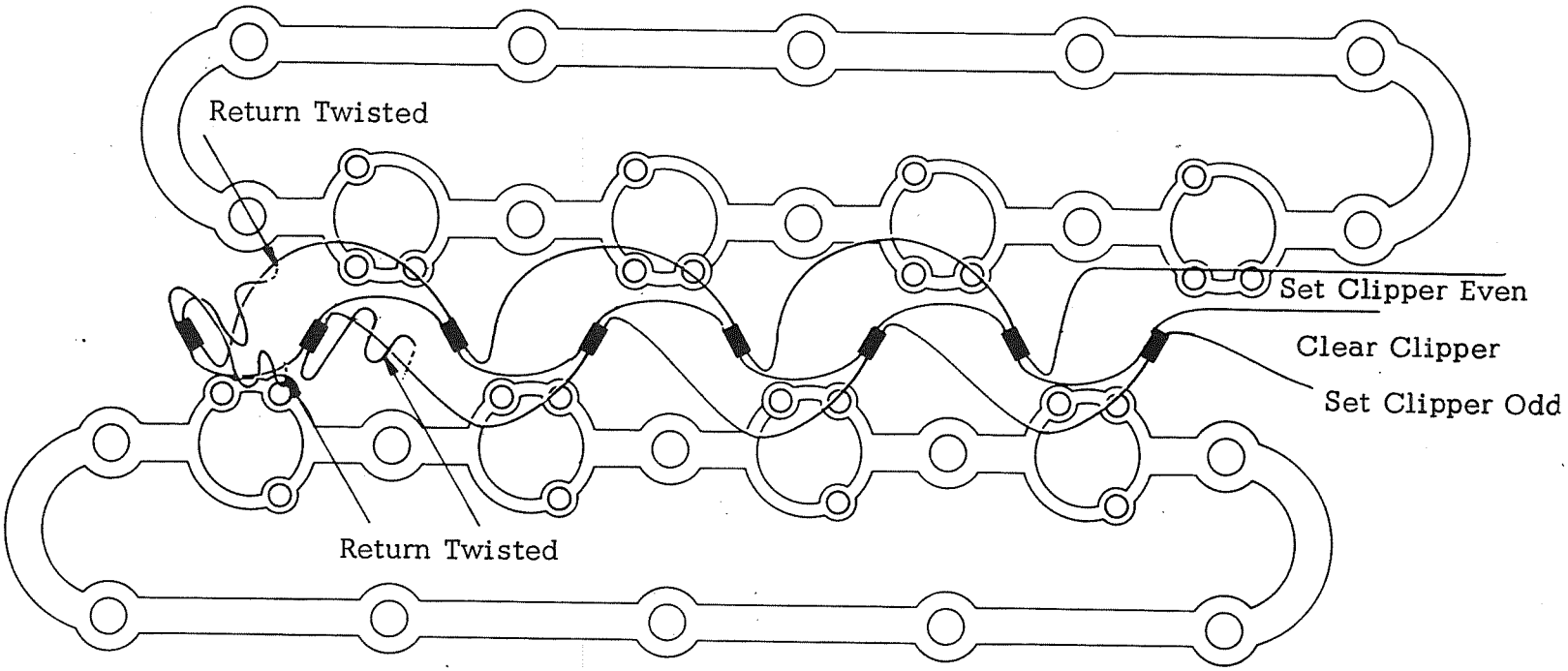


Fig. 23e Clipper Core Windings

structures, the clear windings were also distributed but wound between the drive apertures in the return leg and around the drive apertures elsewhere.

The end-around loop was constructed differently for each ring counter. Each was made as a flat strip transmission line approximately 0.4 inches wide from 0.006 inch thick conductors with lengths up to a maximum of 5.0 inches.

Separate windings were wound to link the appropriate aperture(s) in each stage, ie, leg 1 of the input aperture in each stage was linked by the I1 bias winding. This method of winding provided the flexibility of using individual drivers for each winding or of connecting several windings in series and driving them from a single driver. It was then possible to determine the allowable variation in drive mmf between windings driven at the same clock time.

4.4.2 Pulse Patterns

Operation of the integrated logic registers requires the four clock cycle shown in Fig. 24 clear odd, advance even-to-odd, clear even, and advance odd-to-even.

The pulse widths used were all 3 microseconds measured from the 90% to 90% points. The rise and fall times of the current pulses were approximately 0.1 microseconds. For each structure the individual bias windings, with the exception of the I1 bias winding, were connected in series with the set clipper winding and driven together. The clear windings were similarly connected and driven together. For the major portion of the testing and evaluation, the above windings were driven separately, as were the I1 bias, advance, and flux drive windings. With separately driven windings, the effect on operating range due to varying the current through each winding was determined. Later the advance winding was placed in series with the rest of the bias windings, and a current

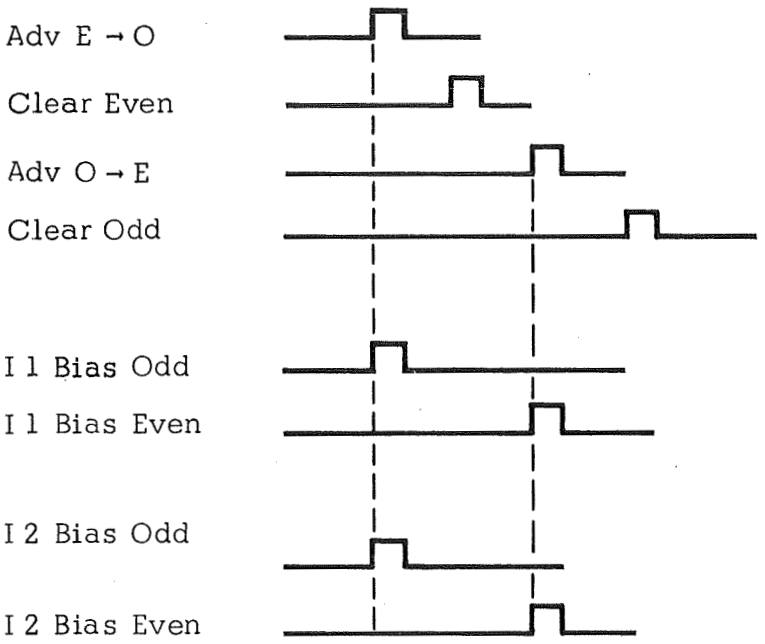


Fig. 24 Pulse Pattern for Logic Structures

divider network was used to pass approximately half of the advance current through the I1 bias winding. Finally, the reduced-size registers were operated, using only four drivers, by connecting the flux drive windings in series with the bias/advance windings. This grouping of windings is shown in Table 9 together with the clock time the windings are driven at.

4.4.3 Circuit Evaluation

The integrated multistage logic circuits were evaluated initially to determine the current required to set different flux levels into a stage, the transfer characteristics for different coupling loop configurations, and the source and magnitude of the transfer losses. The evaluation was completed by measuring flux gain for both isolated stages and the four register stages, by determining signal-to-noise ratios, and by plotting range maps of operating ring counters using different drive winding connections.

Table 9 Register Windings, Connections, and Clock Times

Connection A, for Full and Reduced Size Structures

τ_1	τ_2	τ_3	τ_4
Clear 0	Flux drive 0	Clear E	Flux drive E
Clear 01	Adv E → 0	Clear 01	Adv 0 → E
Clear 02	I1 bias	Clear 02	I1 bias
Clear clipper	I2 bias	Clear clipper	I2 bias
	Set clipper		Set clipper
	Drive aperture bias*		Drive aperture bias*

Connection B, for Full and Reduced Size Structures

Clear 0	Flux drive 0	Clear E	Flux drive E
Clear 01	Adv E → 0	Clear 01	Adv 0 → E
Clear 02	I1 bias	Clear 02	I1 bias
Clear clipper	I2 bias	Clear clipper	I2 bias
	Set clipper		Set clipper
	Drive aperture bias*		Drive aperture bias*

* Full-size structures only

Note: Windings within brackets are connected in series and driven from common current drive source.

Table 9 continued

Connection C, for Reduced Size Structures

τ_1	τ_2	τ_3	τ_4
(Clear 0, Clear 01, Clear 02, Clear clipper)	(Flux drive 0, Adv E → 0, I1 bias, I2 bias, Set clipper)	(Clear E, Clear 01, Clear 02, Clear clipper)	(Flux drive E, Adv 0 → E, I1 bias, I2 bias, Set clipper)

Note: Windings within brackets are connected in series and driven from common current drive source

Figure 25 shows the input current required to set different flux levels into a stage without I 1 bias and as a function of the flux switched by the flux drive, for SR#4, one of the full-size registers tested. In another test the use of I 1 bias was found as expected to merely displace the position of the curves relative to zero input current. This is indicated in the figure by the values of input current enclosed in parentheses.

The experiments relative to coupling loops were made to determine the effects of using a 3:2 turns ratio and a 2:1 turns ratio for the coupling loops. Detailed flux accounting was taken for all legs of both the transmitter and the receiver which are involved in a transfer. The results of these investigations of transfer characteristics and of transfer losses indicated that sufficient coupling loop current could be obtained with the 2:1 turns ratio and that the additional flux available with this ratio would be required.

The early circuits which were evaluated had marginal gain characteristics. This deficiency was traced to excessive leakage flux. The effect of this leakage flux as discussed in section 4.2.4, is to increase the noise signal out of the transmitter. It also reduces both the upper limit of the advance current range and the maximum coupling loop current. Each of these factors influences the gain characteristics of the circuits negatively. After the plated-on eddy current shields were applied to structures used in the registers, the gain characteristics of the circuits materially improved.

A flux gain curve for signal transfer between two stages of operating register SR#6 is shown in Fig. 26. This is seen to have the necessary three crossovers of the unity gain line. The two extreme crossovers are points of stable equilibrium, the middle crossover is a point of unstable equilibrium. Signals below the unstable equilibrium point will decay until they reach the lower stable point and signals greater than the unstable equilibrium point will grow until they reach the upper stable point. When

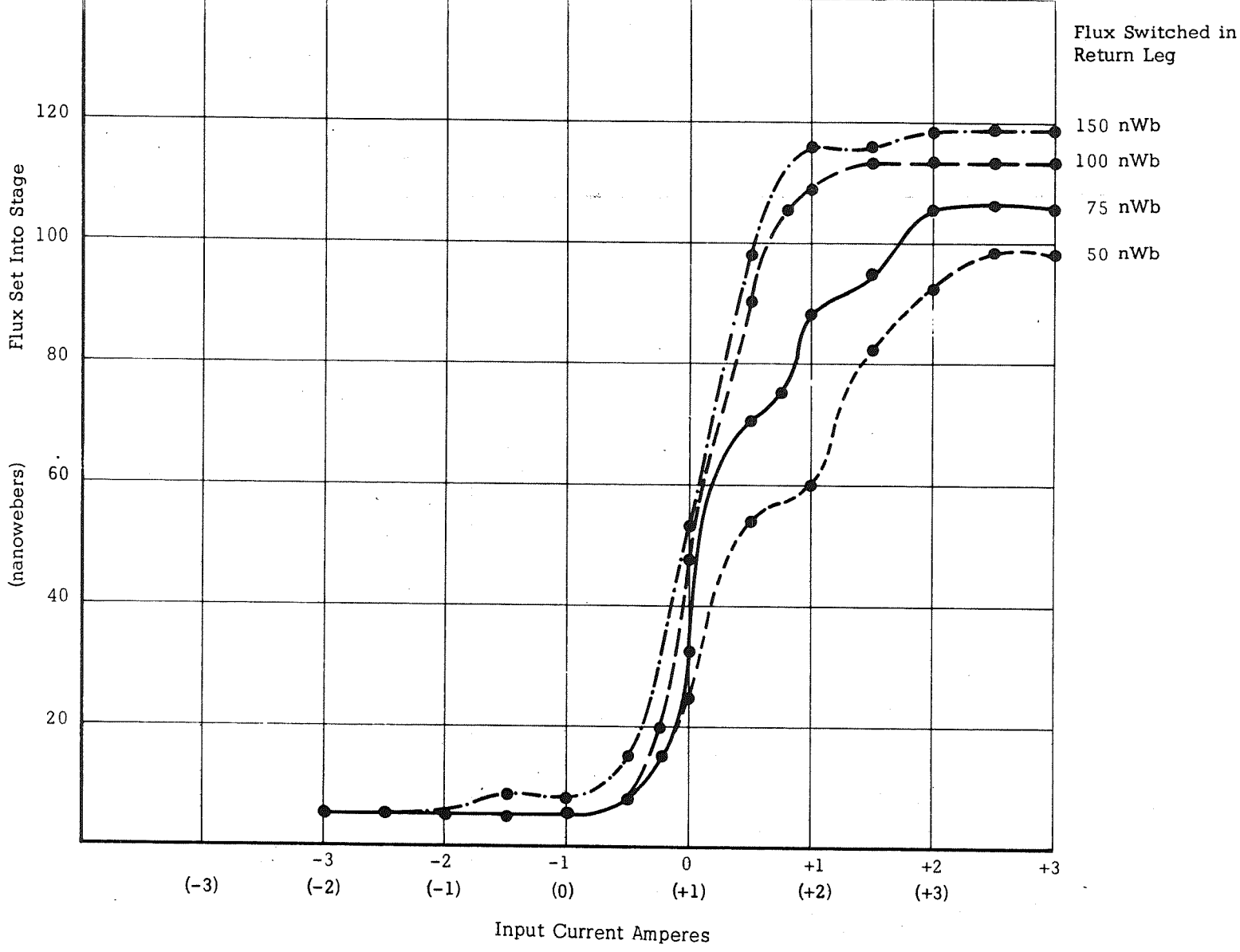


Fig. 25 Flux Set Into a Stage as a Function of Input Current

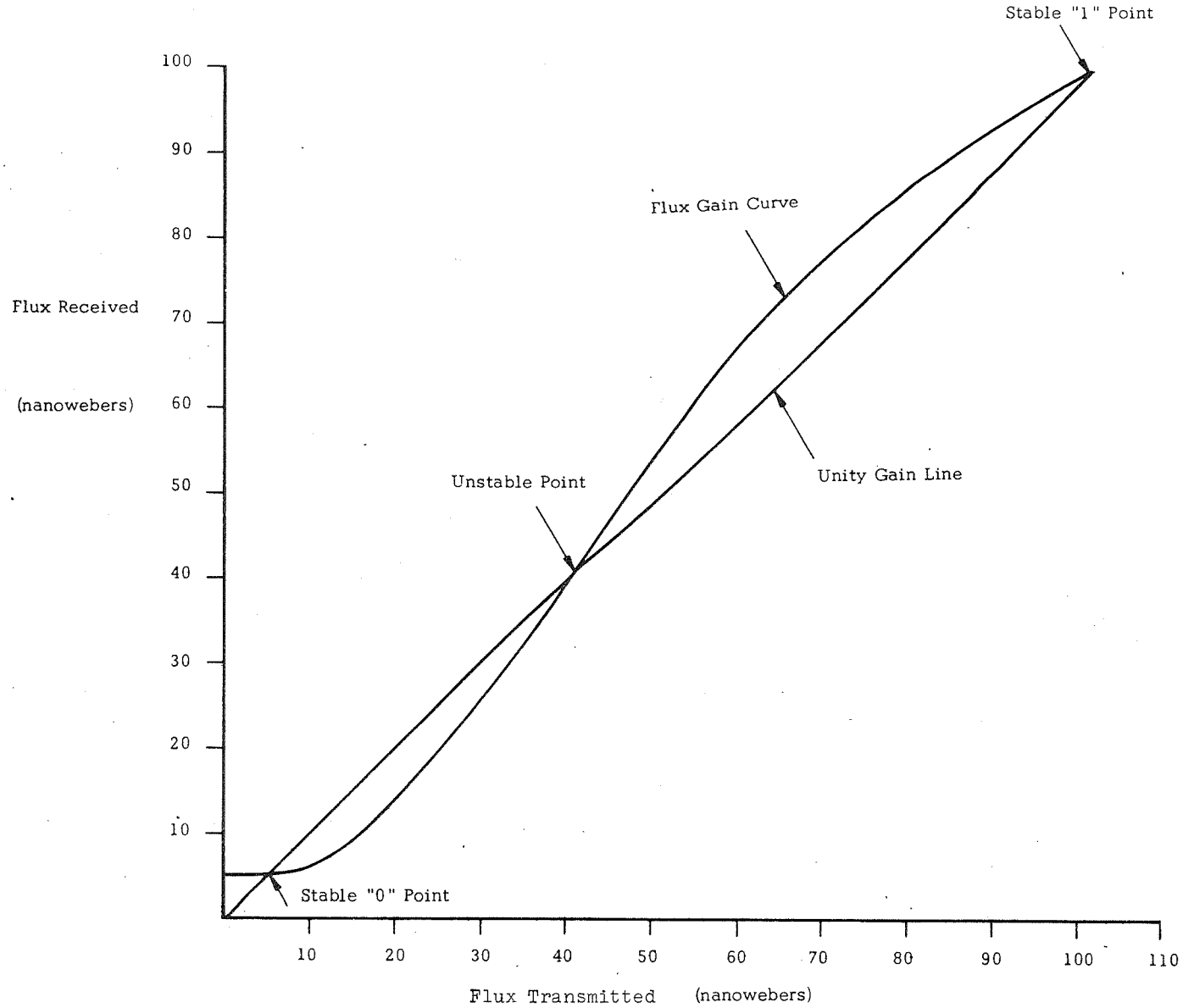


Fig. 26 Flux Gain for a Pair of Isolated Stages of SR #6

all stages of a register have such a gain curve, the curve for the full register is similar but will have a steeper slope through the point of unstable equilibrium.

The signal-to-noise ratio is determined by the flux gain characteristics of the circuits and can be determined from the two stable equilibrium points on the flux gain curve. The flux gain curve, however, varies with operating level of the drive currents. The ratio obtained from a gain curve reflects only the ratio obtainable under the same drive conditions. It is useful to know in addition, the variation of the s/n ratio over the operating range. This is best done by direct measurement. S/n ratios of from 4:1 to 12:1 were measured for individual circuits, registers and ring counters. The highest ratios are obtained in the middle portion of the range.

Range maps were taken for operating ring counters, to determine the variation of advance drive, for different values of I1 bias, over which stable operation could be obtained. Such a range map for SR #6 is shown in Fig. 27. The ratio of I1 bias current to advance current for a line drawn through the end points of the range map is 0.45. By maintaining this current ratio with a current divider, the range is extended to the limits indicated in the range map. Table 10 gives the operating range for advance drives obtained for three winding configurations: separate windings driven by individual drivers, series connection of I1 bias and advance windings driven by a common driver, and series connection of I1 bias, advance and flux drive windings driven by a common driver. This latter case uses only one driver at each clock time. A range map for SR#10 of operation using one driver for each clock time is shown in Fig. 28. SR#10 is seen to have a range of from 2.2 to 3.2 amperes for a variation of both advance currents simultaneously. The signal-to-noise ratio over this range varied from 5:1 to 10:1. The operating range of SR#10 as a function of temperature is given in Table 11.

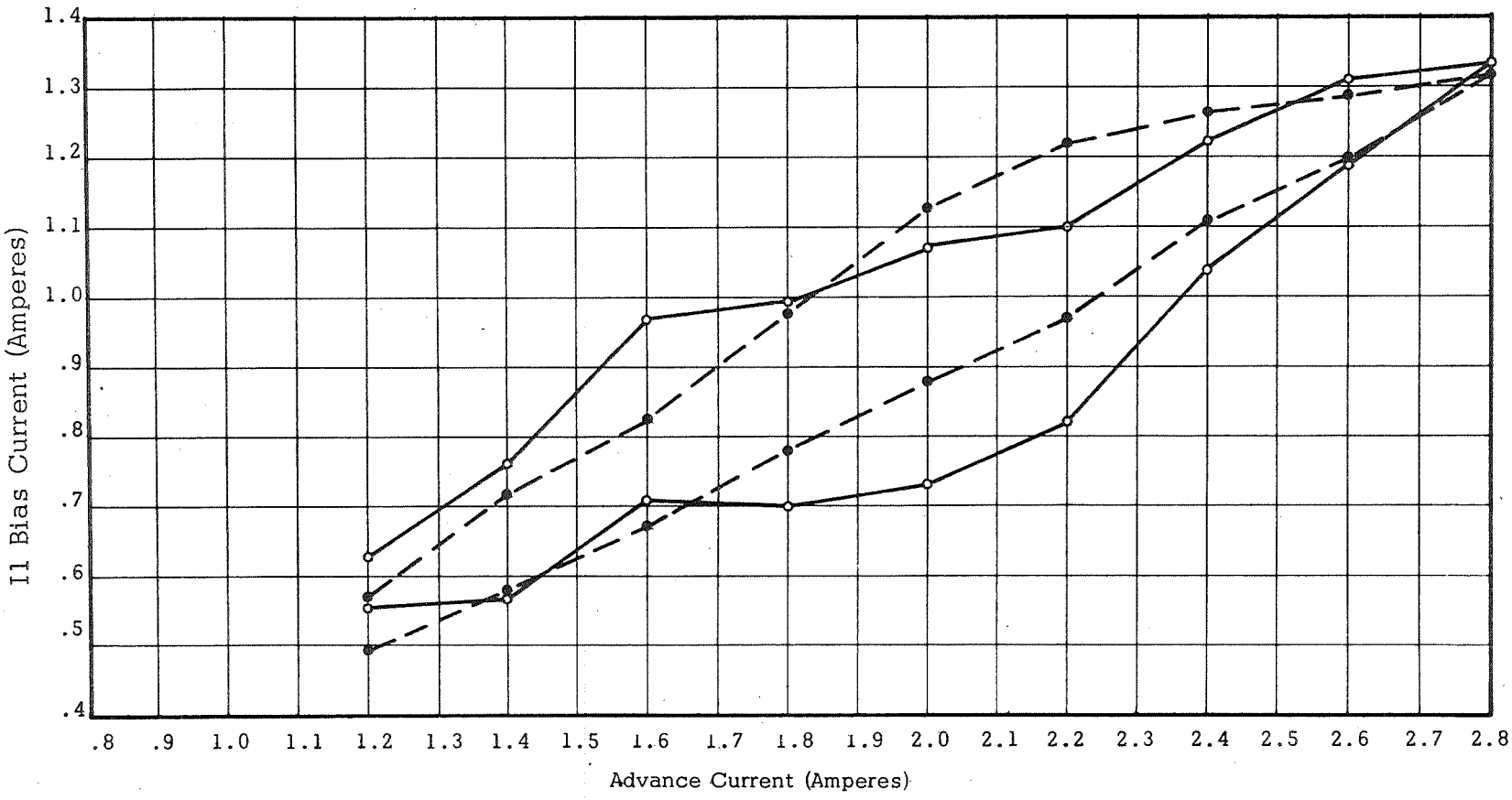


Fig. 27 Range Map for Advance and I1 Bias Currents in SR #6

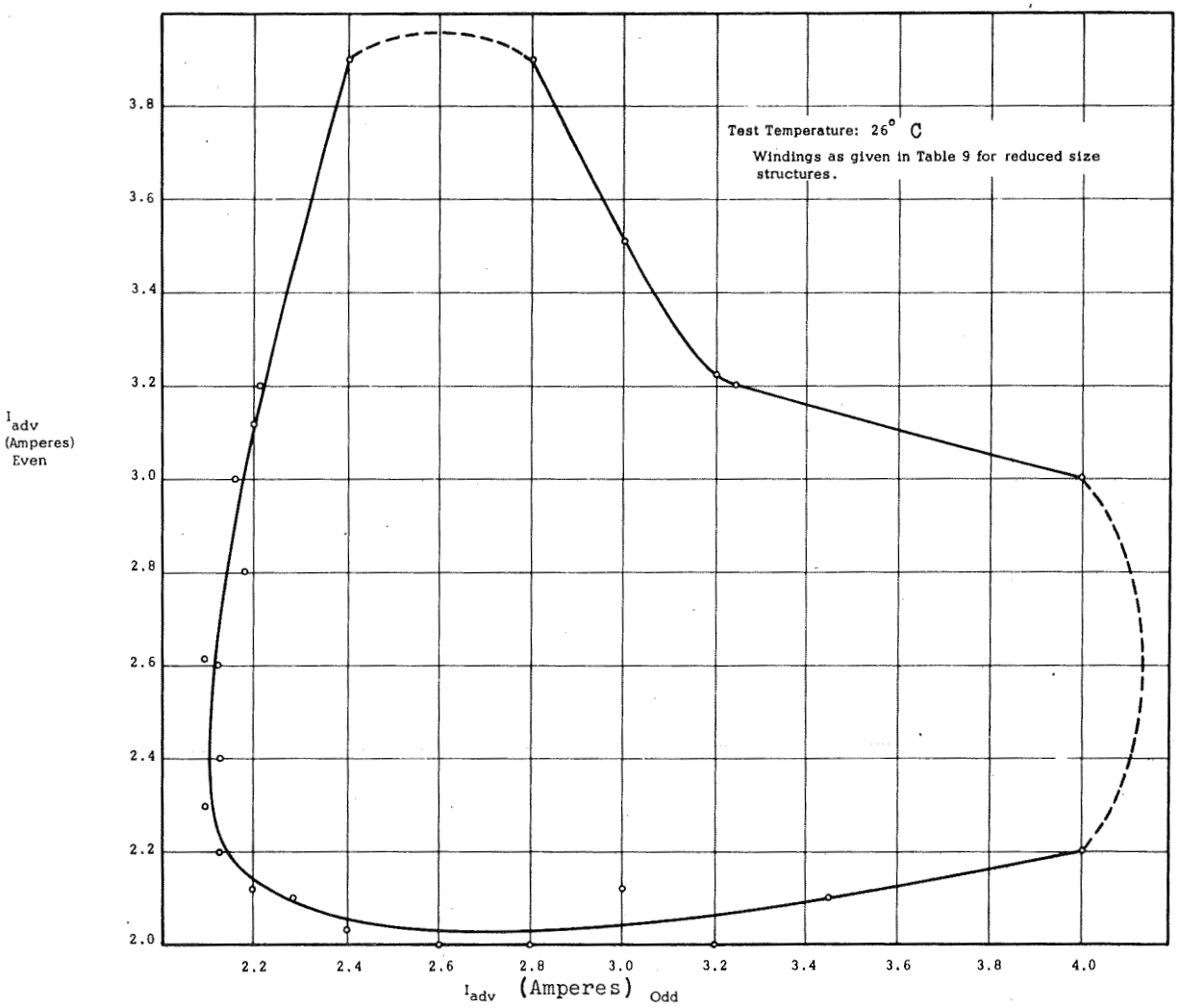


Fig. 28 Range Map of SR #10 for Advance Odd and Advance Even Using One Driver for Each Clock Time

Table 10 Operating Range of Ring Counters

	Separate Windings (Note 1) (Amps)	Series Il Bias and Advance Windings (Note 1) (Amps)	Series Il Bias Advance and Flux Drive Windings (Note 1) (Amps)	Series Il Bias Advance and Flux Drive Windings (Note 2) (Amps)
SR#6	1.4 - 2.3	0.9 - 2.6	-	-
SR#7	1.8 - 2.6	1.0 - 3.4	-	-
SR#8	1.2 - 1.8	0.9 - 2.9	2.0 - 3.6	2.0 - 2.4
SR#10	1.4 - 2.0	0.7 - 2.4	2.1 - 4.1	2.2 - 3.2

Note 1: Range of advance current for all other drives held constant

Note 2: Range of advance current for both odd and even advance currents varying together

Table 11 Operating Range of SR#10 Vs Temperature

Temperature (^{o}C)	Range A (1 (amps)	Range B (2 (amps)	Range C (3 (amps)
0	-	-	-
26	1.0	> 1.9	> 1.9
38	0.5	> 1.9	2.6
60	0.1	0.4	1.5

1) Range for variation of both advance currents in same direction: Worst Case.

2) Range for variation of odd advance current with even advance current held constant.

3) Range for variation of even advance current with odd advance current held constant.

5.0 PLATED CONDUCTORS

A batch type process for applying conductors to logic structures has been developed. In this process the surface of the logic structure is first coated with the desired conductor pattern using a conducting ink. After curing, the conductor pattern is overplated with copper to the desired thickness. Possible interactions that would affect the magnetic characteristics were checked for at each stage of the process. After completion of the plating, the structures were tested using the plated conductors.

To evaluate this process single-stage structures were used. A two-turn pattern was painted through the output aperture of each structure with a gold ink. This pattern is shown in Fig. 29. The ink was cured at 300°C to form a conducting pattern. After curing, the pattern was overplated first with 0.002" of copper, and then, after testing, the plating was continued to a thickness of 0.004". Figure 30 shows a photograph of a single-stage structure with plated-on two-turn conductors. In Fig. 31 the profile characteristics of the output aperture of a single-stage structure with plated two-turn conductors are shown for -20°C, +20°C, and +60°C. Table 12 summarizes the profile characteristics of five single-stage structures for the three temperatures. The data were taken using the plated two-turn conductors and bipolar current drivers. For comparison, at room temperature, the characteristics taken with the test jig are also listed.

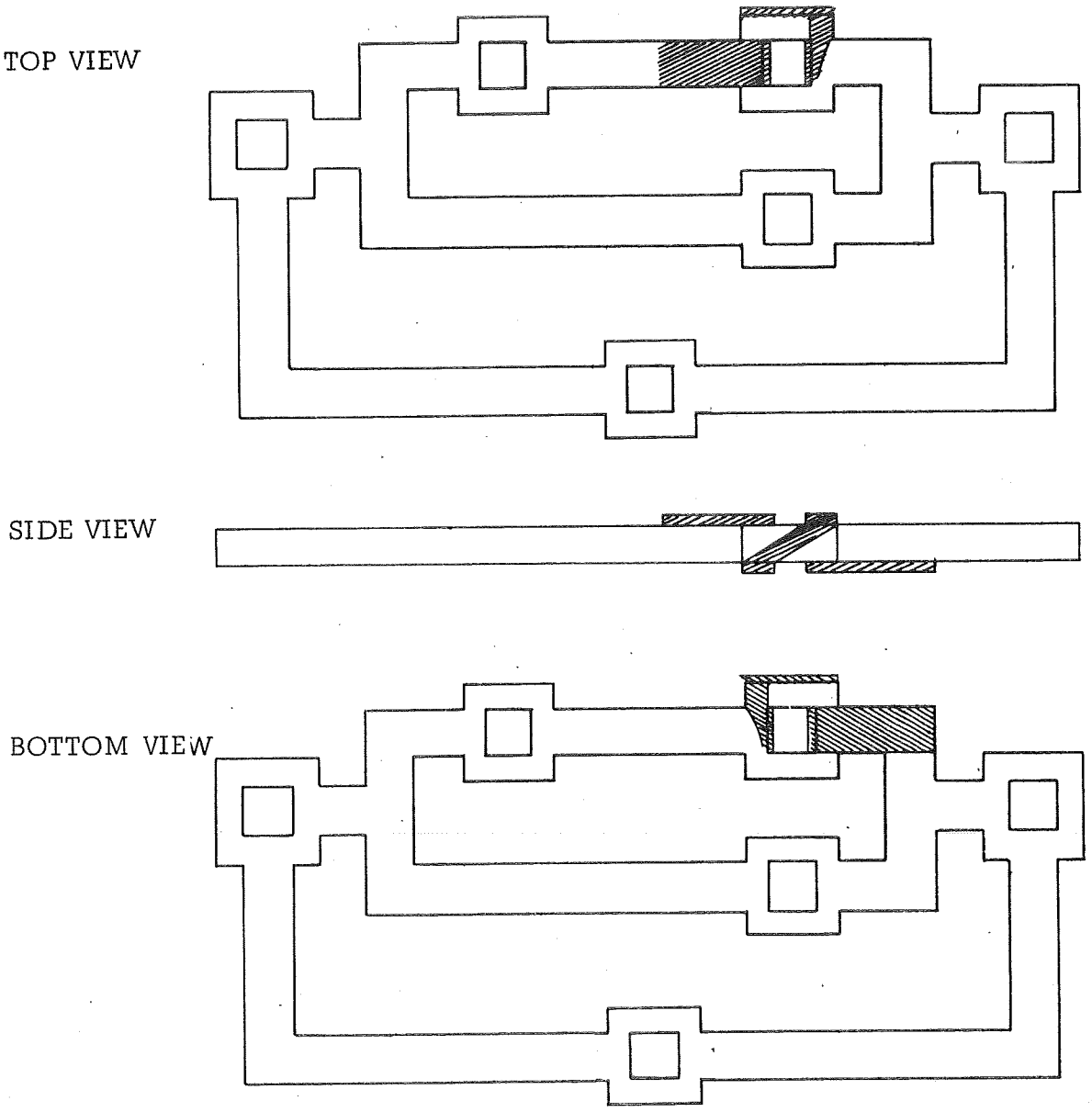


Fig 29 Pattern for Plated-On Conductors

The tests have shown that the process does not alter the magnetic characteristics of logic structures which have had plated two-turn conductors applied, and that the conductors adhere to the surface of the structures without setting up magnetostrictive strains. Conductors so applied are joint free, the only connections being those required to connect to the drive circuits. It is interesting to note that the joint-free conductors are formed even though the original pattern is applied at different times and therefore contains junctions. This allows considerable freedom in the process, including correction of imperfections found in the pattern by inspection after curing the ink prior to final plating.

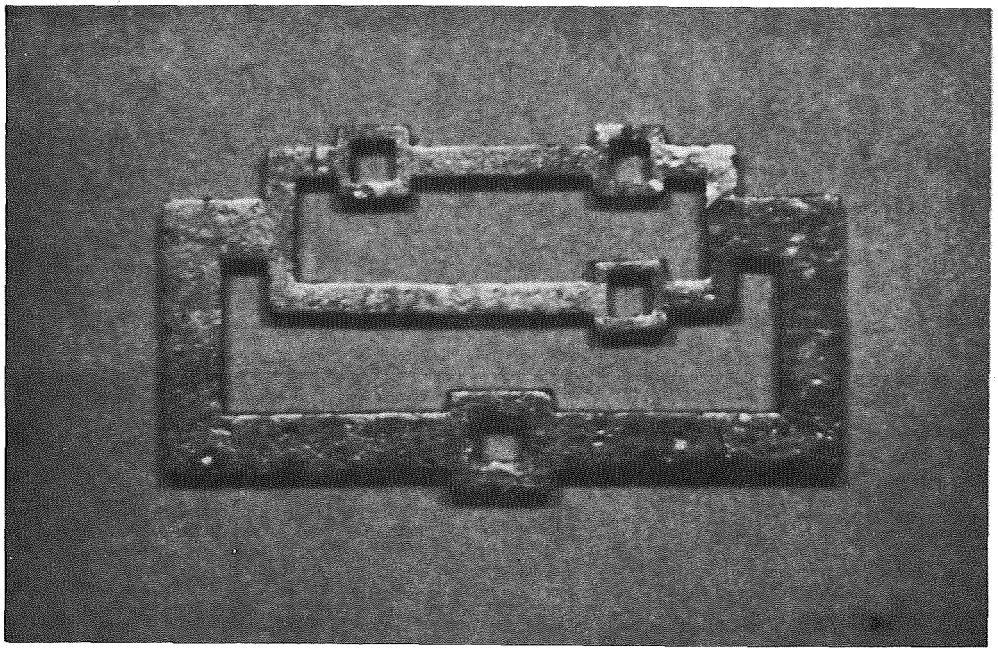
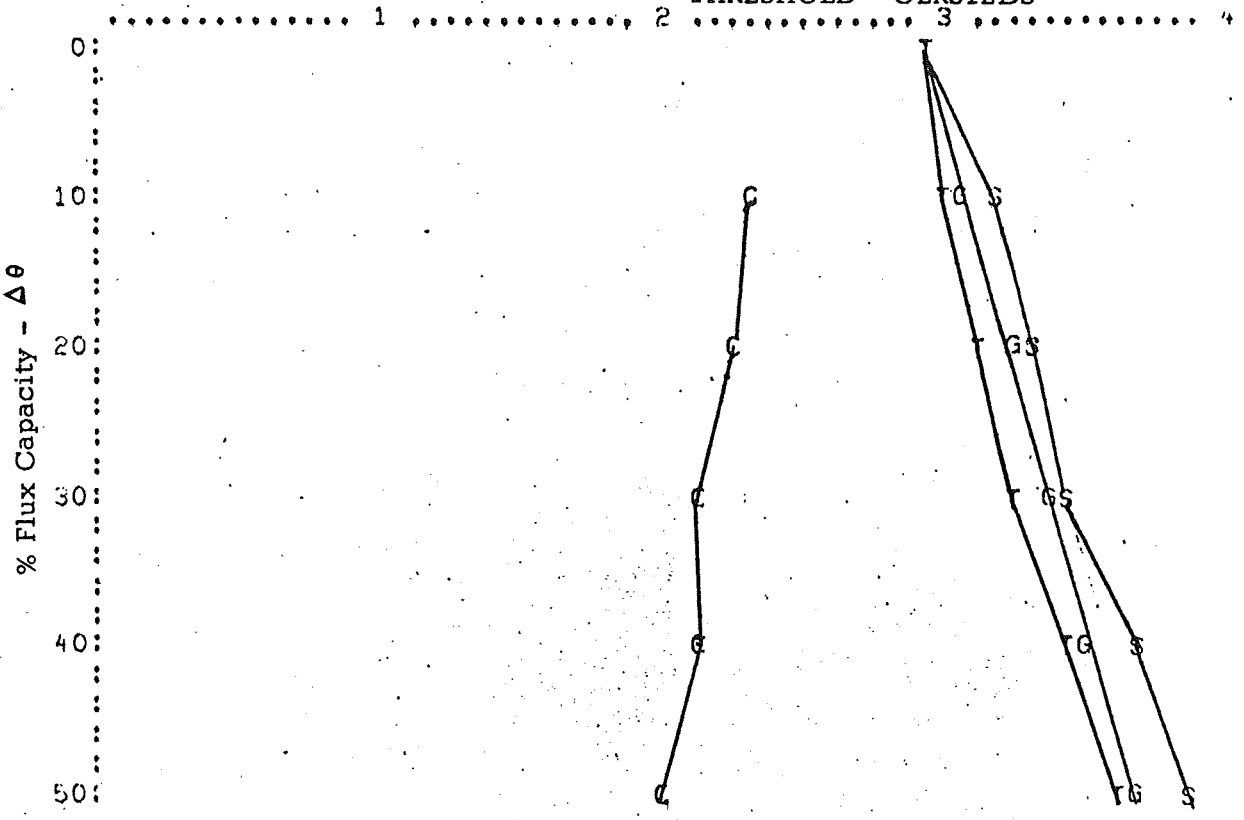


Fig. 30 Single-Stage Structure with Plated-On Conductors

IS 25 326-1023 / 0.062 FIRING TEMP = 1300
CORE NUMBER 32 N2 TEMP = 1300

THE SCALE FOR THE ABSCISSA IS 2 PERCENT PER LINE.
THE SCALE FOR THE ORDINATE IS 0.063 OERSTEDS PER SPACE (1 OERSTED EQUALS 16 SPACES).



THE CORE DIAMETER IN INCHES IS	0.062
THE CORE MATERIAL IS	IS 25-326
THE FIRING NUMBER IS	1023
THE CORE NUMBER IS	32
THE FIRING TEMP IS	1300
THE N2 TEMP IS	1300

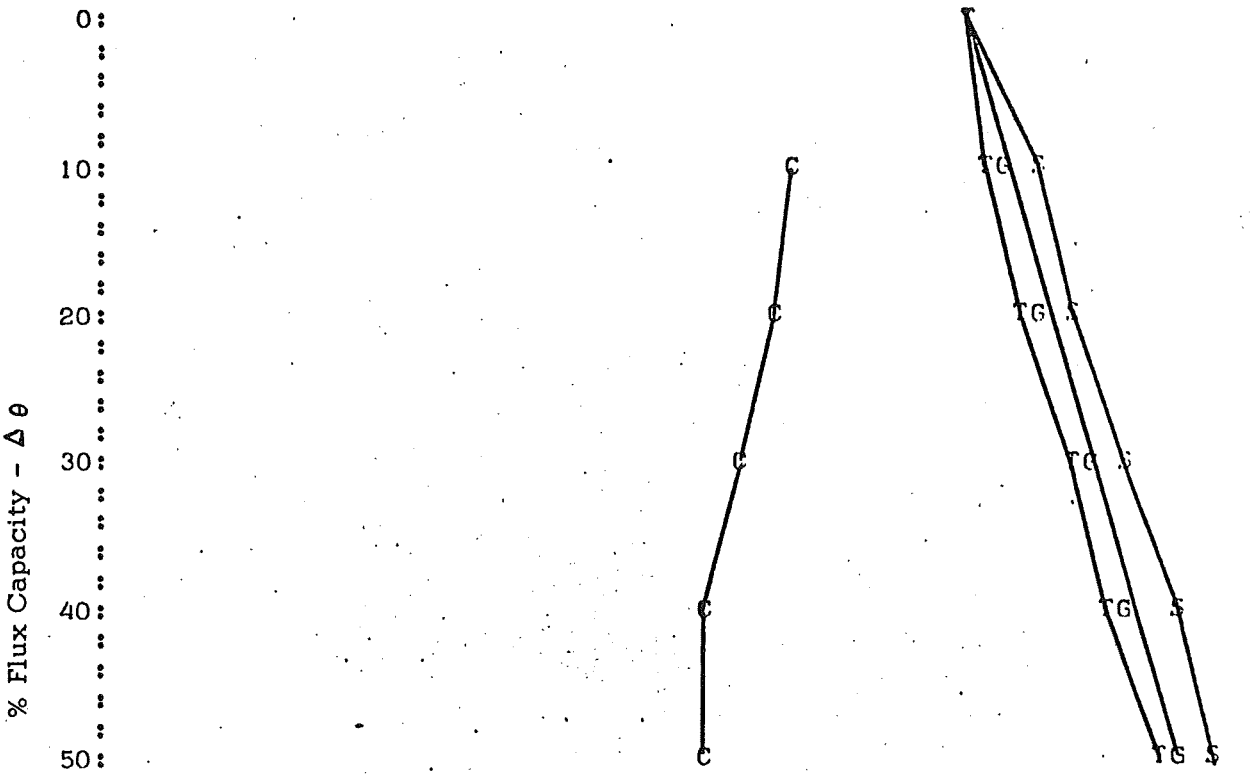
TH = 2.885 OERSTEDS
TH(PS) = 3.810 OERSTEDS....FOR DEL. θ = 50 PERCENT
TH(PC) = 1.910 OERSTEDS....FOR DEL. θ = 50 PERCENT
TH(PS)/G(50) = 1.063
TH(PC)/G(50) = 0.533
TH(PC)/TH = 0.662

% Δφ	TH:SET		TH(PS)		TH(PC)	
	OER.	A.T.	OER.	A.T.	OER.	A.T.
0	2.885	1.136				
10	2.951	1.162	3.099	1.220	2.261	0.890
20	3.053	1.202	3.241	1.276	2.159	0.850
30	3.180	1.252	3.393	1.336	2.068	0.814
40	3.353	1.320	3.602	1.418	2.052	0.808
50	3.541	1.394	3.810	1.500	1.910	0.752

Fig. 31a Profile Characteristics of Output Aperture With Plated-On Conductors at - 20°

IS 25 326-1023 / 0.062 FIRING TEMP = 1300
CORE NUMBER 32 N2 TEMP = 1300

THE SCALE FOR THE ABSCISSA IS 2 PERCENT PER LINE.
THE SCALE FOR THE ORDINATE IS 0.050 OERSTEDS PER SPACE (1 OERSTED EQUALS 20 SPACES). THRESHOLD - OERSTEDS



THE CORE DIAMETER IN INCHES IS 0.062
THE CORE MATERIAL IS IS 25-326
THE FIRING NUMBER IS 1023
THE CORE NUMBER IS 32
THE FIRING TEMP IS 1300
THE N2 TEMP IS 1300

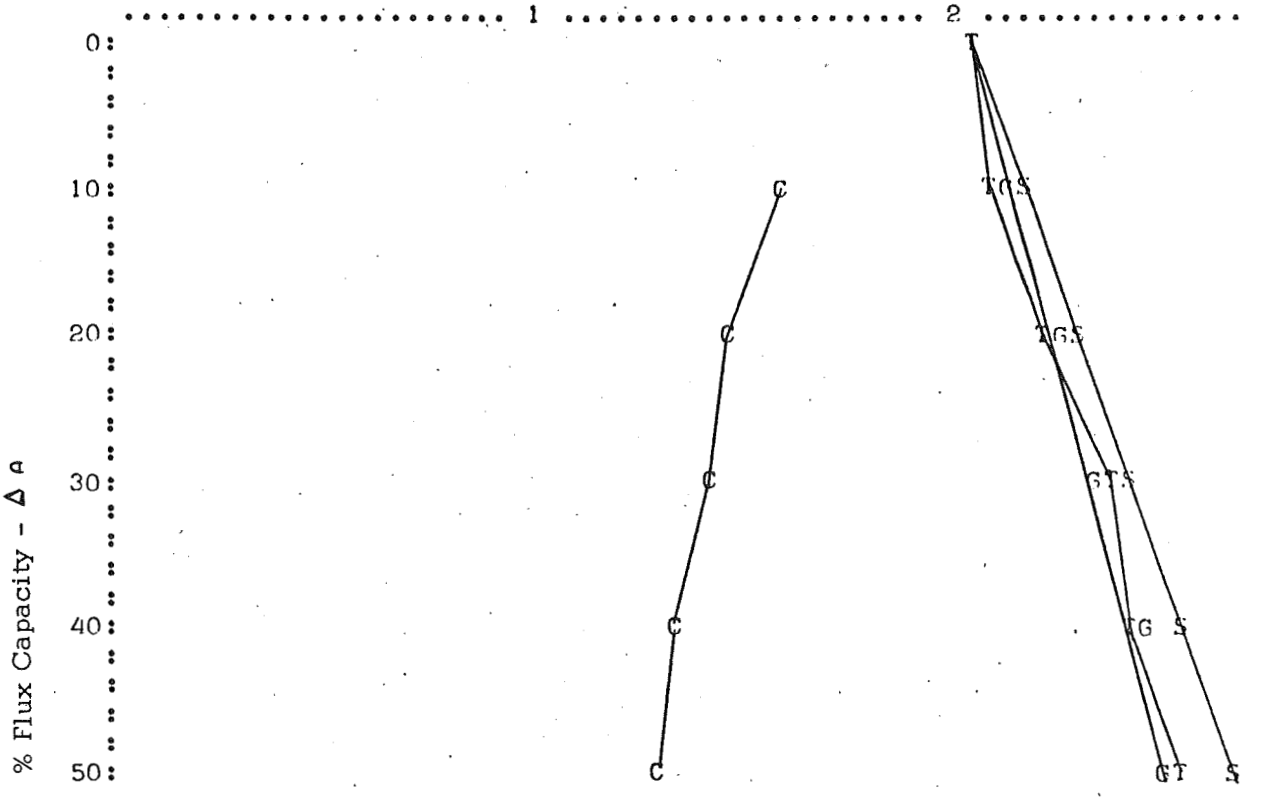
TH = 2.388 OERSTEDS
TH(PS) = 3.119 OERSTEDS....FOR DEL. 0 = 50 PERCENT
TH(PC) = 1.666 OERSTEDS....FOR DEL. 0 = 50 PERCENT
TH(PS)/G(50)= 1.052
TH(PC)/G(50)= 0.562
TH(PC)/TH = 0.698

% Δφ	TH:SET		TH(PS)		TH(PC)	
	OER.	A.T.	OER.	A.T.	OER.	A.T.
0	2.388	0.940				
10	2.469	0.972	2.586	1.018	1.895	0.746
20	2.560	1.008	2.687	1.058	1.829	0.720
30	2.692	1.060	2.840	1.118	1.753	0.690
40	2.824	1.112	3.007	1.184	1.671	0.658
50	2.946	1.160	3.119	1.228	1.666	0.656

Fig. 31b Profile Characteristics of Output Apertures With Plated - On Conductors at 25°C

326-1023 / 0.062 FIRING TEMP = 1300
CORE NUMBER 32 N2 TEMP = 1300

THE SCALE FOR THE ABSCISSA IS 2 PERCENT PER LINE.
THE SCALE FOR THE ORDINATE IS 0.042 OERSTEDS PER SPACE (1 OERSTED EQUALS 24 SPACES).



THE CORE DIAMETER IN INCHES IS	0.062
THE CORE MATERIAL IS	IS 25-326
THE FIRING NUMBER IS	1023
THE CORE NUMBER IS	32
THE FIRING TEMP IS	1300
THE N2 TEMP IS	1300

TH = 1.986 OERSTEDS
TH(PS) = 2.626 OERSTEDS....FOR DEL. 0 = 50 PERCENT
TH(PC) = 1.260 OERSTEDS....FOR DEL. 0 = 50 PERCENT
TH(PS)/G(50)= 1.065
TH(PC)/G(50)= 0.511
TH(PC)/TH = 0.634

% Δφ	TH:SET		TH(PS)		TH(PC)	
	OER.	A.T.	OER.	A.T.	OER.	A.T.
0	1.986	0.782				
10	2.052	0.808	2.134	0.840	1.524	0.600
20	2.149	0.846	2.225	0.876	1.433	0.564
30	2.286	0.900	2.372	0.934	1.372	0.540
40	2.362	0.930	2.484	0.978	1.295	0.510
50	2.484	0.978	2.626	1.034	1.260	0.496

Fig. 31c Profile Characteristics of Output Aperture with Plated-On Conductors at 60°C

Table 12 Threshold Vs Temperature: Single-Stage Logic Structures Having Plated 2-Turn Conductors

Specimen	Parameter	Temperature (^{o}C) -20 *	+20/RT *	+20/RT ‡	+60 *
P1	TH	2.9	2.4	2.3	2.0
"	TH_{ps}	3.8	3.1	3.1	2.6
"	TH_{pc}	1.9	1.7	1.6	1.3
P2	TH	2.9	2.4	2.3	2.0
"	TH_{ps}	3.8	3.2	3.1	2.6
"	TH_{pc}	2.0	1.6	1.6	1.3
P3	TH	2.8	2.3	2.3	1.9
"	TH_{ps}	3.8	3.1	3.0	2.5
"	TH_{pc}	1.9	1.5	1.5	1.2
P4	TH	2.8	2.2	2.2	1.8
"	TH_{ps}	3.7	3.0	2.9	2.5
"	TH_{pc}	1.9	1.5	1.4	1.1
P5	TH	2.8	2.3	2.3	1.9
"	TH_{ps}	3.8	3.1	3.0	2.5
"	TH_{pc}	1.9	1.6	1.5	1.2

* Data taken using plated conductor

‡ Data taken using test jig

} All values in oersteds rounded off to nearest tenth

6.0 ARITHMETIC PROCESSOR

The design of a serial arithmetic processor based on the integrated magnetic logic structures has been investigated. The multistage integrated logic structures wired as shift registers form the sum and addend registers. The logic functions of OR, AND and Negation are readily formed with the integrated logic structure designs used in the full-size and reduced-size multistage structures. Although these functions are sufficient for designing an arithmetic unit, the number of stages and the complexity of the interconnections make a design based on the use of an additional logic structure, the exclusive-OR, attractive. The exclusive-OR produces the function $(A+B) \cdot \overline{A \cdot B}$

The function $(A+B) \cdot \overline{A \cdot B}$ is the sum function of a half adder[4]. A full serial adder can be formed from two half adders. A logic design for a serial adder unit which is compatible with magnetic logic circuits is shown in Fig. 32. Here a majority circuit is used to form the carry function. The two cascaded exclusive - OR circuits form the sum function. The augend and addend are initially stored in the A and B registers. After addition the sum is stored in the A register.

The A and B registers are formed from integrated structures connected as shift registers. The majority circuit and carry delay loop circuits are also formed from the integrated structures. The exclusive -OR function is formed from an exclusive -OR structure.

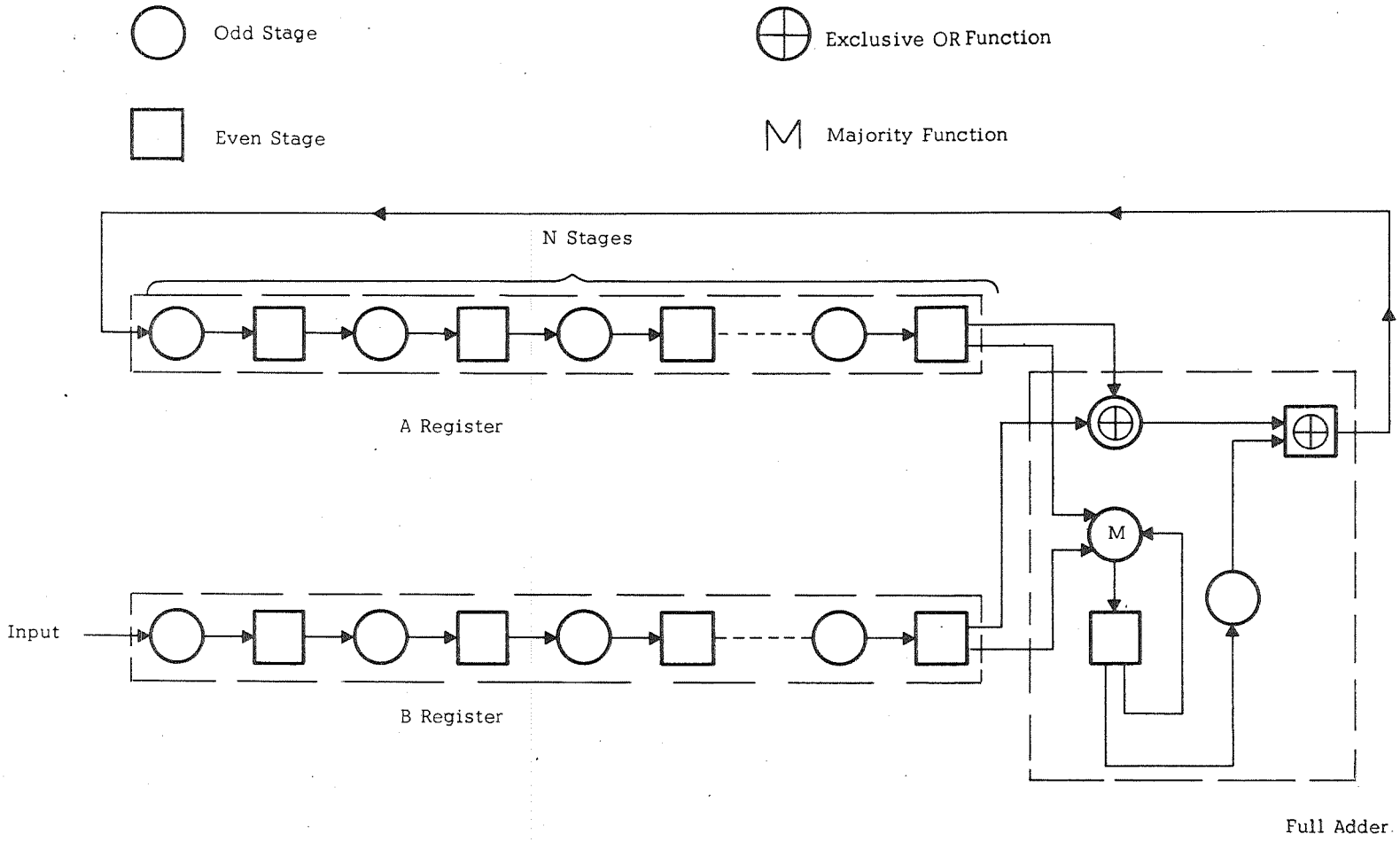


Fig. 32 Basic Adder Unit Based on Integrated Multistage Logic Structures

This basic addition unit modified to add or subtract both positive and negative numbers is shown in Fig. 33. Logic for this arithmetic unit is based on the ONE's complement method of subtraction[5]. The registers are extended to be three stages longer than the input word length: one stage to accommodate the larger number of sum bits, one for the sign bit and one for the sign bit overflow. An additional exclusive -OR stage has been added to the B register to provide for complementing negative numbers on input. The input stage for the A register has also been modified to provide for the end-around carry. The time sequence of operation for this arithmetic unit is:

1. Clear A register and input augend* into B register.
2. Cycle augend from B register into A register. Input addend* into B register.
3. Add contents of B register to contents of A register. Store sum in A register.
4. Set ONE into carry delay loop for overflow of sign bit.
5. Add contents of carry delay loop to contents of A register.
6. Read sum output from A register.

The exclusive -OR structure on which the arithmetic unit is based is shown in Fig. 34. The design is similar to one stage of the reduced-size structure with the exception of the extra aperture in leg A forming an aperture pair. Two basic winding configurations are of special interest. In one, Configuration A shown in Fig. 34a, the input winding threads each aperture of the aperture pair in an opposite direction, ie, down through one aperture and back up through the other. A special feature of this input configuration is that it is polarity independent. The second configuration uses only one input aperture and the drive aperture. Each input links both one leg of the input aperture and leg 1 of the drive aperture. Two variations of this configuration are shown in Figs. 35b and c. The clear state and flux states for the four

*Complement if negative number

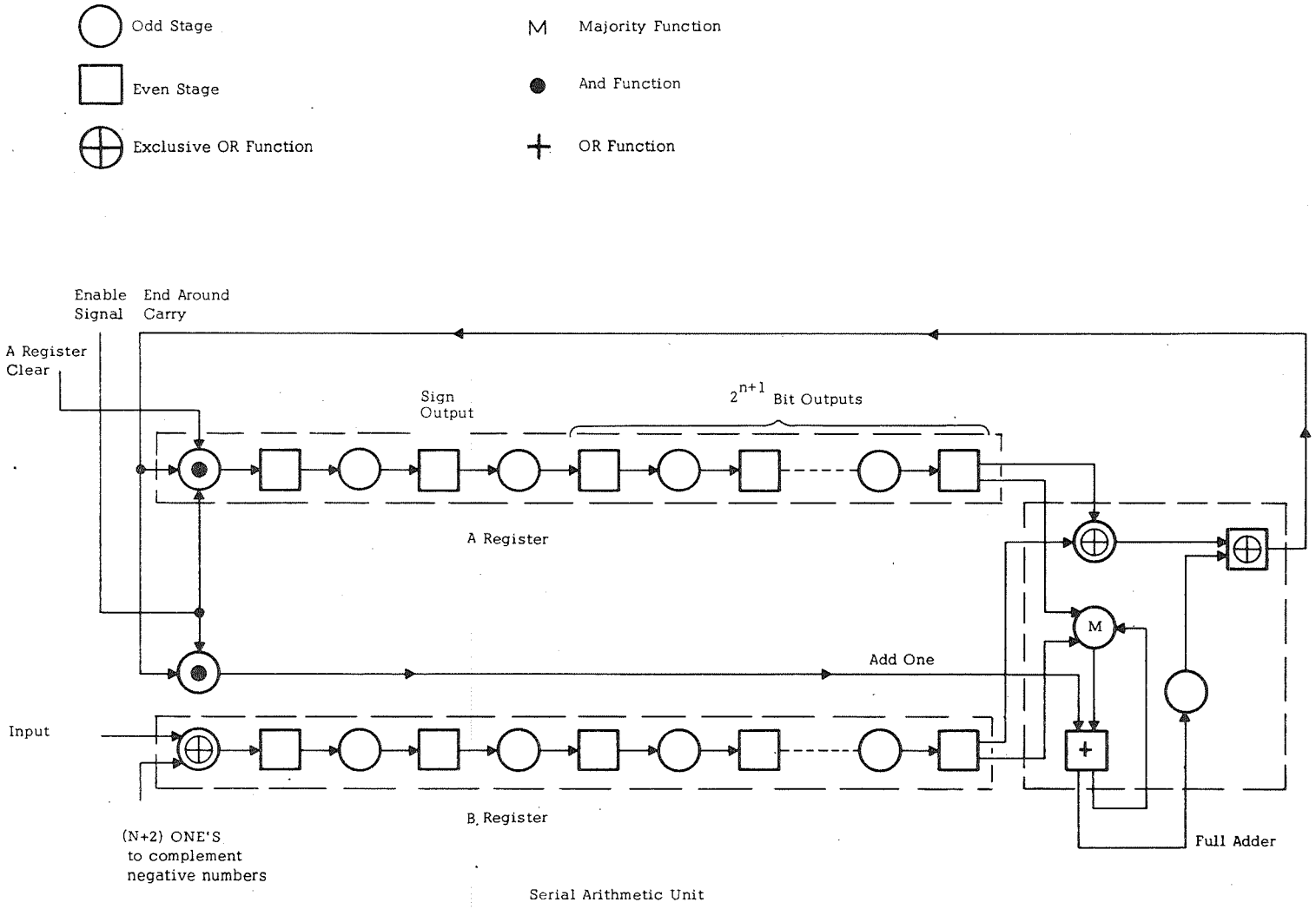


Fig. 33 Arithmetic Unit Based on Integrated Multistage Logic Structures

Fig. 34 Exclusive -OR Logic Structure

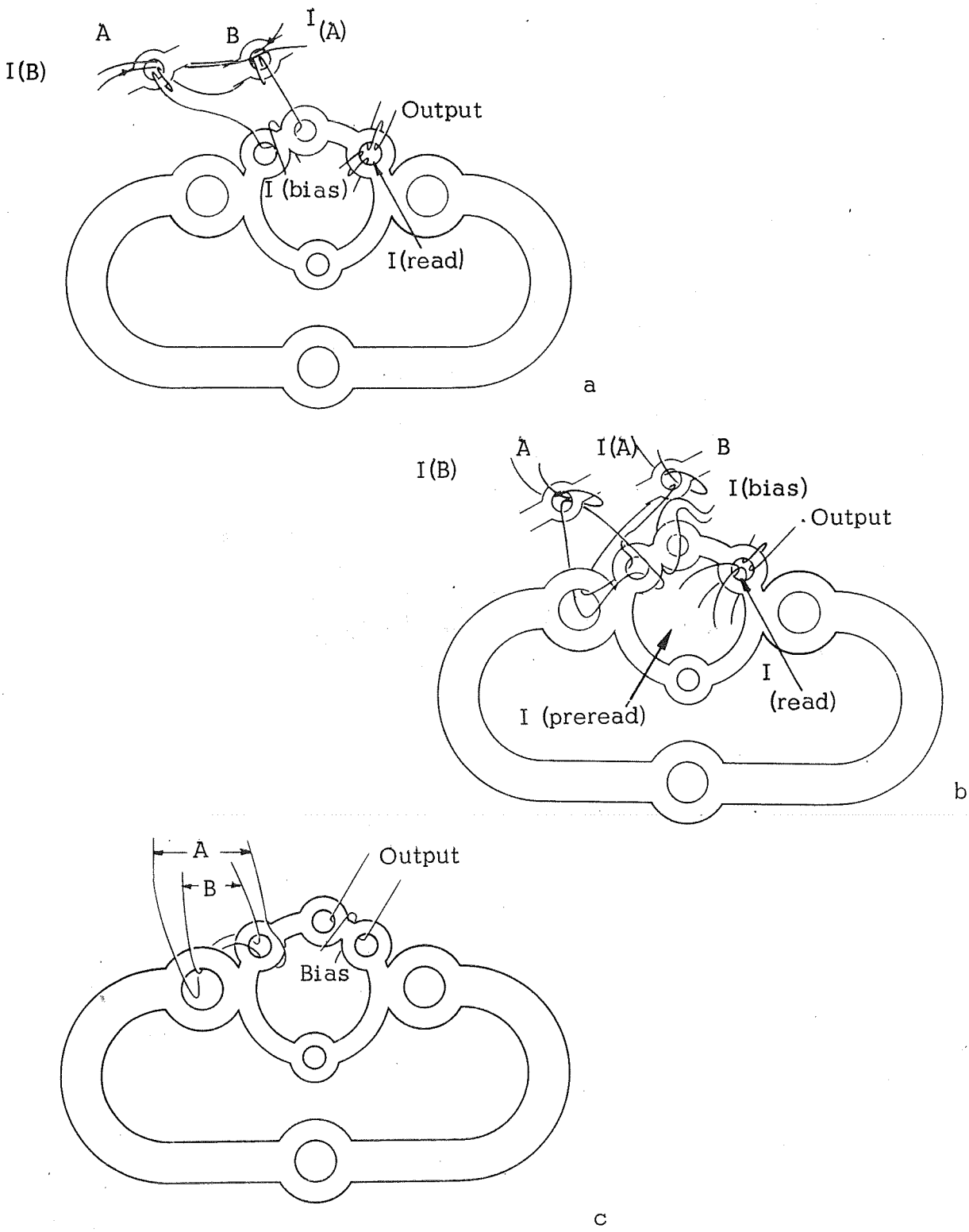
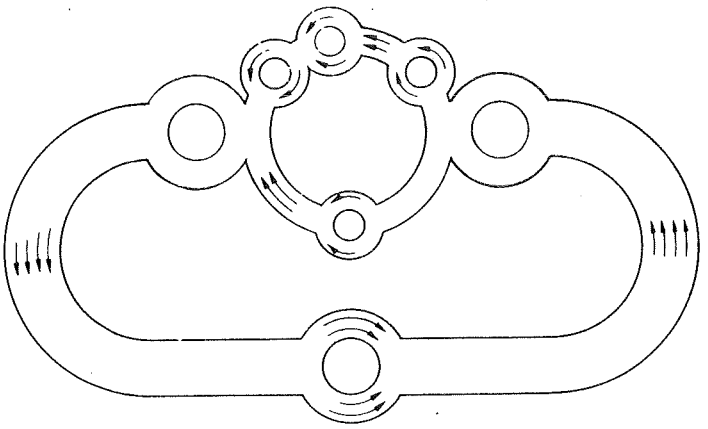


Fig. 35 Exclusive -OR Winding Configurations

input combinations are shown in Figs 36a through e for the winding configuration of Fig. 35a. The flux states in legs A and B are the same for the winding configurations of Fig. 35b and c[∓] except for the function A · B which is shown in Fig. 36f. Note that for the function A·B the output aperture is blocked for both configurations, but in one case by leg A remaining in the clear state and in the other by leg A being fully switched. This latter case requires that the output be taken from the aperture pair to prevent inducing currents in the output winding during the switching of leg A.

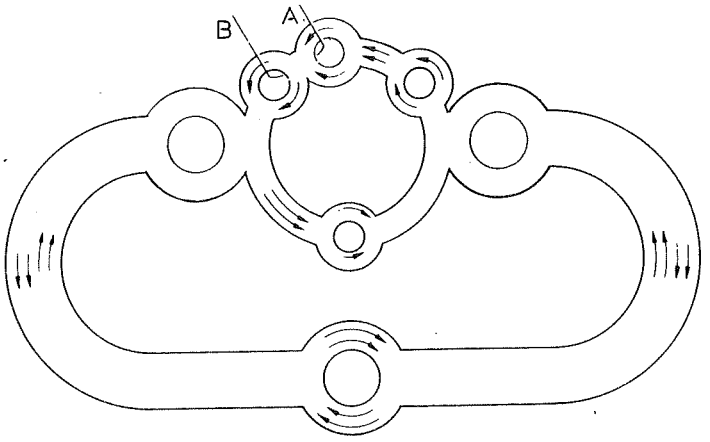
The exclusive -OR structures were evaluated at room temperature. The signals of the input variables were provided from 50/80 size toroidal cores each having a flux of approximately 100 nWbs. The ONE to ZERO ratios produced at the output aperture were measured for several operating conditions producing ONE signals greater than 80 nWbs. The test conditions used are given in Table 13. for the test data presented in Table 14. The ONE to ZERO ratio at the output of the exclusive -OR structure varied between 2.25:1 to 7:1 depending upon the operating conditions.

∓ The drive aperture is used only for decoupling the exclusive -OR stage when the transmitter stages are cleared. Therefore the flux pattern around the output apertures is not changed by the clearing of the transmitter stages. Also the flux states for the four input combinations are determined only by the direction of the currents through the input aperture.



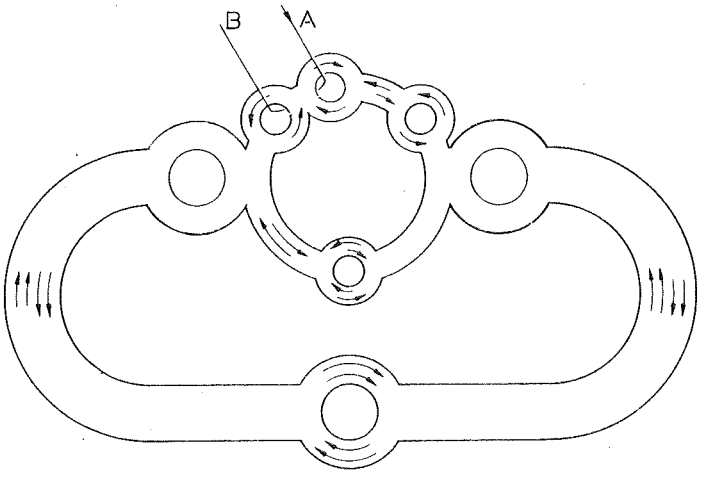
Clear State

a



$\bar{A} \cdot \bar{B}$

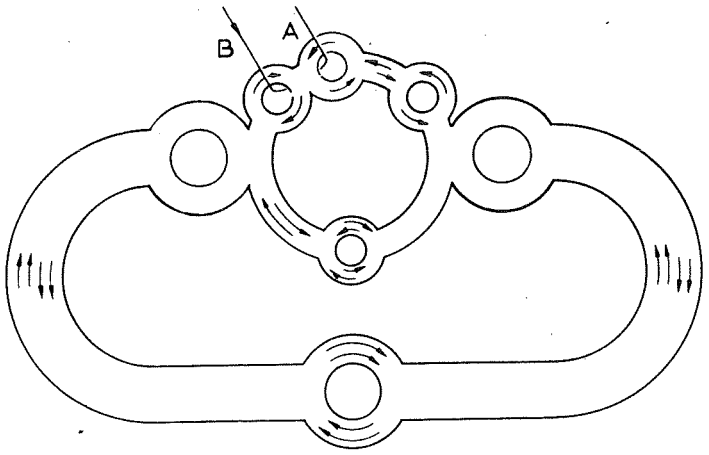
b



$A \cdot \bar{B}$

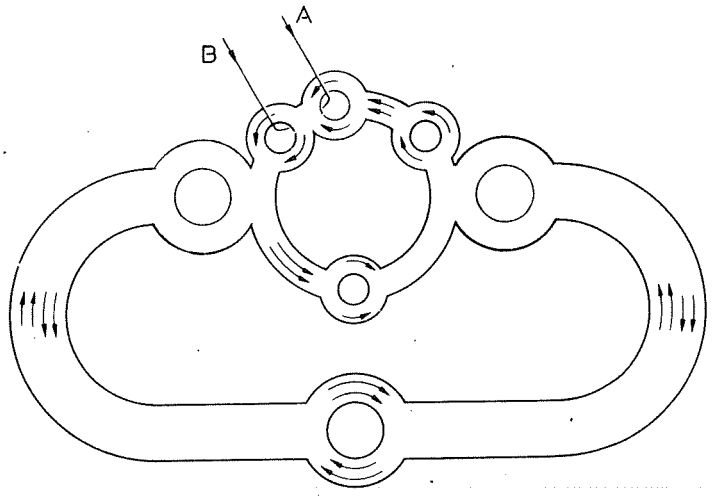
c

Fig. 36 Exclusive -OR Flux States



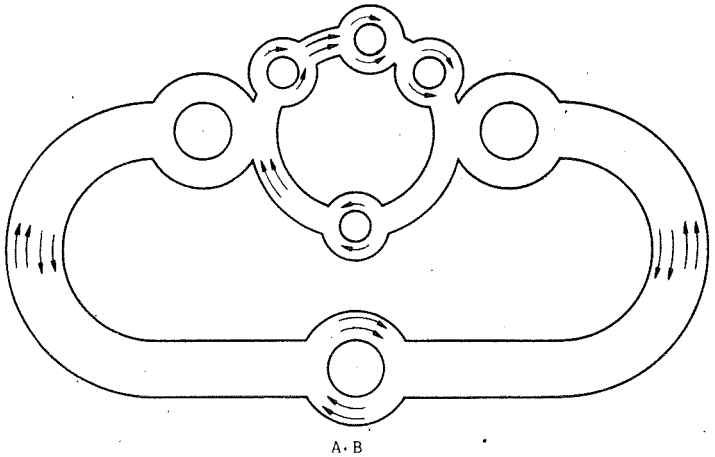
$\bar{A} \cdot B$

d



$A \cdot B$

e



$A \cdot B$

f

Fig. 36 Continued

Table 13 Drive Conditions for Exclusive - OR Tests

Drive	Configuration A Current			Configuration B Current			Configuration C Current	
	Turns (No.)	Cond.I (amps)	Cond.II (amps)	Turns (No.)	Cond.I (amps)	Cond. II (amps)	Turns (No.)	Cond. I (amps)
I(Clear)	8	4.0	4.0	8	3.8	3.8	8	3.9
I(flux drive)	3	3.0	3.5	3	1.85	1.85	3	3.0
I(bias	1	0.62	0.80	1	0.1	0.1	1	0.25
I(A)	2	2.5	2.0	2	2.1	1.25	2	1.8
I(B)	2	2.5	2.0	2	2.2	1.25	2	1.8
I(pre read)	-	-	-	1	0.8	0.8	-	-
I(read)	2	1.0	1.0	1		0.8	1	1.1

All pulse widths, 3 msec.

Table 14 Exclusive OR Test Data Winding Configuration A

Condition I

Function	Output Flux (nWb)	Leg A Flux (nWb)	Input A Flux ∓ (nWb)	Input B Flux ∓ (nWb)
$A \cdot \overline{B}$	110	100	80	-
$\overline{A} \cdot B$	105	100	-	80
$A \cdot B$	15	15	110	120
$\overline{A} \cdot \overline{B}$	15	10	-	

Condition II

Function	Output Flux (nWb)	Leg A Flux (nWb)	Input A Flux ∓ (nWb)	Input B Flux ∓ (nWb)
$A \cdot \overline{B}$	80	70	80	-
$\overline{A} \cdot B$	80	70	-	80
$A \cdot B$	15	12	110	120
$\overline{A} \cdot \overline{B}$	15	10	-	-

∓ A two turn coupling loop through a single 50/80 core was used for each input signal.

Table 14 Exclusive -OR Test Data Winging Configuration B

Condition I

Function	Output Flux (nWb)	Leg A Flux (nWb)	Input A Flux* (nWb)	Input B Flux* (nWb)
$A \cdot \overline{B}$	90	115	175	
$\overline{A} \cdot B$	90	110		185
$A \cdot B$	30	185	170	150
$\overline{A} \cdot \overline{B}$	10	10	-	-

Condition II

Function	Output Flux (nWb)	Leg A Flux (nWb)	Input A Flux* (nWb)	Input B Flux* (nWb)
$A \cdot \overline{B}$	90	120	190	-
$\overline{A} \cdot B$	90	115	-	205
$A \cdot B$	40	200	190	175
$\overline{A} \cdot \overline{B}$	10	10	-	-

Winding Configuration C

Condition I

Function	Output Flux (nWb)	Leg A Flux (nWb)	Input A Flux* (nWb)	Input B Flux* (nWb)
$A \cdot \overline{B}$	90	125	230	-
$\overline{A} \cdot B$	90	125	-	200
$A \cdot B$	25	210	235	175
$\overline{A} \cdot \overline{B}$	15	20	-	-

* A single turn coupling loop through two 50/80 cores was used for each input signal.

7.0 CONCLUSIONS/RECOMMENDATIONS

The goals of this project have been achieved. Integrated multistage logic structures in both the full size and the reduced size have been fabricated, tested and operated as shift registers and ring counters with good range and good signal-to-noise ratio. Two-turn conductors have been applied through the output aperture by a batch type of plating process without altering the magnetic characteristics of the structures. An arithmetic unit based on the integrated multistage logic structures has been designed and the special logic structure required by the design, an exclusive-OR structure, has been designed, fabricated and two configurations have been tested. The investigations which have been made in pursuit of these goals have shown that the integration of two materials in the logic structures has improved the circuit performance and provided additional design flexibility. The process used to apply the plated conductor pattern has been extended to apply plated-on eddy current shields to the integrated multistage logic structures. These shields have effectively reduced the leakage flux, resulting in more nearly theoretical circuit operation.

The following areas are recommended for further investigation.

1. Modification of the integrated logic structure design to permit the complete wiring of circuits by the plating process.
2. Extension of the conductor-plating process to provide multilayer conductor patterns.

3. Development of a material for the integrated structures with a lower value of H_c.

4. Extension of the use of low H_c material to other magnetic paths in the logic structures.

APPENDIX I

SPECIMEN IDENTIFICATION

Full-Size Structures

Specimen ID	High H_c	Low H_c	Firing No.*	Core No.*
F1	IS-25-34-8	IS-40-18-1	1539	66
F2	"	"	1554	61
F3	"	"	"	62
F4	"	"	1562	63
F5	IS-25-34-9	"	1594	61
F6	"	"	"	64
F7	IS-25-34-9	IS-40-18-1	1594	62
F8	IS-25-28	IS-40-7-1	948	61
F9	IS-25-28-3	IS-40-7-1	957	61
F10	IS-25-34-9	IS-40-18-1	1604	61

Reduced-Size Structures

Specimen ID	High H_c	Low H_c	Firing No. *	Core No.
R1	IS-25-51-7	IS-40-18-2	1821	82
R2	IS-25-51-7	IS-40-18-2	1821	81
R3	IS-25-50-6	IS-40-18-2	1829	83
R4	IS-25-50-1	IS-40-18-2	1789	82
R5	IS-25-53-2	IS-40-18-2	1841	82
R6	IS-25-53-2	IS-40-18-2	1841	81
R7	IS-25-53-2	IS-40-18-2	1846	81
R8	IS-25-50-3	IS-40-18-2	1841	84
R9	IS-25-52-1	IS-40-18-2	1843	81
R10	IS-25-53-2	IS-40-18-2	1846	84

* Each structure is uniquely identified by the combination of the firing number and the core number.

SPECIMEN IDENTIFICATION

Plated Conductor Pattern on Single Stage Structure

Specimen ID	High H_c	Firing No. *	Core No. *
P1	IS 25-32-6	1023	32
P2	"	"	35
P3	IS 25-32-1	1245	34
P4	"	"	35
P5	"	1252	34

* Each structure is uniquely identified by the combination of the firing number and the core number.

APPENDIX II

ASSAY AND ANALYSIS OF TRACE IMPURITIES OF STARTING MATERIALS

Fe_2O_3

C.K. Williams Co. Cat. No. R2199R

	Lot No. 8 Percent
Fe	99.3
Si	0.015
Mn	0.08
Mg	0.015
Al	0.006
Mo	<0.005
Cu	<0.001
Ni	0.007
Ca	0.025
Cr	0.002

$MgCO_3$

J. T. Baker Chemical Co. Cat. No. 2432

	Lot No. 25325 Percent	Lot No. 33328 Percent
Assay (as MgO)	43.0	42.7
Insoluble in HCl	0.003	0.005
Chloride (Cl)	0.002	0.001
Sulfate (SO_4)	0.001	0.002
Calcium (Ca)	0.005	0.02
Heavy Metals (as Pb)	0.0004	0.0005
Iron (Fe)	0.001	0.001
Water Soluble Salts	0.04	0.40

$MnCO_3$

J. T. Baker Chemical Co. Cat. No. 2536

	Lot No. 22632 Percent	Lot 33171 Percent
Assay (as Mn)	44.6	44.9
Insoluble in HCl	0.002	0.002
Chloride (Cl)	0.01	0.020
Sulfate (SO_4)	0.002	0.002
Substances not precipitated by $(NH_4)_2S$ (as SO_4)	0.08	0.08
Other Heavy Metals (as Pb)	0.002	0.004
Iron (Fe)	0.001	0.002
Zinc	0.05	0.010

CdO

J.T. Baker Chemical Co. Cat. No. 1234

	Lot No. 33411 Percent
Assay (CdO)	99.4
Insoluble in CH_3COOOH	0.010
Chloride (Cl)	0.002
Nitrate (NO_3)	0.002
Sulfate (SO_4)	0.005
Copper (Cu)	0.001
Iron (Fe)	0.0005
Lead (Pb)	0.005
Substances not precipitated by H_2S(as SO_4)	0.17

$Ca(CH_3COO)_2$

J.T. Baker Chemical Co. Cat. No. 1266

	Lot No. 26676 Percent
Assay ($Ca(CH_3COO)_2 \cdot H_2O$)	100.2
Insoluble in HCl and NH_4OH precipitate	0.001
pH of 5% solution at 25°C	7.7
Chloride (Cl)	0.0005
Sulfate (SO_4)	0.007
Nitrogen Compound (as N)	0.002
Barium (Ba)	0.001
Heavy Metals (as Pb)	0.0005
Iron (Fe)	0.0001
Magnesium and Alkalies (as SO_4)	0.10

REFERENCES

1. Heckler, C.H, "Development of a Toroid Having Unique Partial Switching Characteristics and Fabrication of an Integrated Magnetic Logic Structure," Final Report Contract NASI-5963, Stanford Research Institute, Menlo Park, Calif. November 1966.
2. Rajchman, J.A. and Lo, A.W., "The Transfluxer - A Magnetic Gate With Stored Variable Setting," RCA Review, vol. 16, June 1955, pp 303-311.
3. Bennion, Crane and Nitzan, "Digital Magnetic Logic," McGraw-Hill, N.Y., 1969.
4. Malvino and Leach, "Digital Principles and Applications", McGraw Hill, N. Y. 1969
5. Phister, Montgomery, Jr., "Logical Design of Digital Computers," John Wiley & Sons, N. Y., 1958.